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Guidelines for Printed Board Component Mounting

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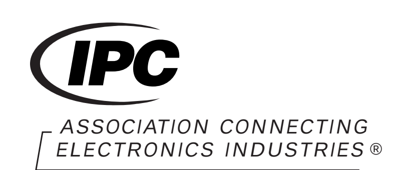
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Guidelines for Printed Board Component Mounting

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Users of this publication are encouraged to participate in the development of future revisions.

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Guidelines for Printed Board Component Mounting

1 SCOPE

This document provides information for preparation of components for assembly to printed boards, contains a review of some pertinent design criteria, impacts and issues, techniques of general interest for assembly (both manual and machines) and discusses considerations of, and impacts upon, subsequent soldering, cleaning, and coating processes. The information herein consists of compiled data representing commercial and industrial applications.

This section discusses general recommended assembly guidelines. Later sections discuss information concerning specific packaging types.

Sections 2 through 5 provide guidelines for the specific component within each sectional document. The parts are described in detail and each section outlines specifics affecting the part class. The descriptions and classifications provided are those generally used in the industry with reference to military and commercial applications.

Due to the rapid progress and evolution in packaging and assembly technology today, this document may not cover all currently available components or assembly techniques such as lead free.

1.1 Purpose The purpose of this document is to illustrate and guide the user seeking answers to questions related to accepted, effective methods of mounting components to printed wiring boards.

1.2 Classification of Board Types and Assemblies

1.2.1 Performance Classes Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there could be an overlap of equipment between classes. These performance classes are the same for both bare boards and assemblies. The printed board user has the responsibility to determine the class to which his product belongs. The contract shall specify the performance class required and indicate any exceptions to specific parameters, where appropriate.

Class 1 – General Electronic Products

Includes consumer products, some computers and computer peripherals suitable for applications where cosmetic imperfections are not important and the major requirement is the function of the completed electronic assembly.

Class 2 – Dedicated Service Electronic Products

Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required and for which uninterrupted service is desired but not critical. Certain cosmetic imperfections are allowed.

Class 3 – High Performance Electronic Products

Includes the equipment and products where continued performance or performance-on-demand is critical, such as in life support items or flight control systems. Equipment downtime cannot be tolerated and must function when required. Assemblies in this class are suitable for applications where high levels of assurance are required, service is essential, or the end-use environment may be uncommonly harsh.

1.2.2 Producibility Levels IPC standards usually provide three design complexity levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore, progressive increases in fabrication cost. These levels are:

- Level A – General Design Complexity - Preferred
- Level B – Moderate Design Complexity - Standard
- Level C – High Design Complexity - Reduced Producibility

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility is for any feature. The specific requirement for any feature that must be controlled on the end item should be specified on the master drawing of the printed board or the printed board assembly drawing.

These levels for assemblies are:

- Level A – Through-hole component mounting only.
- Level B – Surface mounted components only.
- Level C – Simplistic through-hole and surface mounting intermixed assembly.

- Level X – Complex intermixed assembly, through-hole, surface mount, fine pitch and BGA.
- Level Y – Complex intermixed assembly, through-hole, surface mount, ultra fine pitch and chip scale.
- Level Z – Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, and TAB.

1.2.3 Product Types It is important to understand the complex relationship between board types and assembly classifications. The term ''board'' no longer refers just to rigid boards. It now includes single-sided, double-sided and multilayer boards made from rigid, flexible, rigid-flex combinations or boards with high-density microvia dielectric material combinations.

This guideline recognizes that printed boards and printed board assemblies are subject to classifications by intended end item use and other designations based on assembly characteristics. Classification of producibility is related to complexity of the design and the precision required to produce the particular printed board or printed board assembly. Any producibility level or producibility design characteristic may be applied to any end-product equipment category. Therefore, a high-reliability product designated as Class 3 (see 1.2.2) could require Level A design complexity (preferred producibility) for many of the attributes of the printed board or printed board assembly.

1.2.3.1 Rigid Board Types The following rigid board types are classified in IPC-2222 and IPC-6012, *Design and Qualification and Performance Specification for Rigid Printed Boards:*

- Type 1: Single-Sided Printed Board.
- Type 2: Double-Sided Printed Board.
- Type 3: Multilayer Board without Blind or Buried Vias.
- Type 4: Multilayer Board with Blind and/or Buried Vias.
- Type 5: Multilayer Metal-Core Board without Blind or Buried Vias.
- Type 6: Multilayer Metal-Core Board with Blind and/or Buried Vias.

1.2.3.2 Flexible Printed Boards The following flexible printed board types are classified in IPC-2223 and IPC-6013, *Qualification and Performance Specifications for Flexible Printed Boards:*

- Type 1: Single-sided flexible printed wiring containing one conductive layer, with or without stiffeners.
- Type 2: Double-sided flexible printed wiring containing two conductive layers with plated-through holes, with or without stiffeners.
- Type 3: Multilayer flexible printed wiring containing three or more conductive layers with plated-through holes, with or without stiffeners.
- Type 4: Multilayer rigid and flexible material combinations containing three or more conductive layers with plated-through holes.
- Type 5: Flexible or rigid-flex printed wiring containing two or more conductive layers without plated-through holes.

1.2.3.3 PC Card Printed Boards PC Card printed boards are classified by IPC-2224, *Sectional Standard for Design of PWBs for PC Cards.*

1.2.3.4 Single-Chip and Multichip Printed Boards Single chip and multichip printed boards are classified in IPC-2225 and IPC-6015, *Design and Qualification and Performance Specification from Organic Multichip Module Mounting and Interconnecting Structures.*

1.2.3.5 High Density Interconnect Printed Boards The following HDI printed board types are classified in accordance with IPC-2226 and IPC-6016, Design Qualification and Performance Specification for High Density Interconnect (HDI):

- Type I – 1 [C] 0 or 1 [C] 1 with through-vias from surface to surface.
- Type II – 1 [C] 0 or 1 [C] 1 with through-vias buried in the core and from surface to surface.
- Type III – Greater/equal 2 [C] greater/equal to 0.
- Type IV – P greater/equal to 0 where P is a passive substrate with no electrical connecting functions.
- Type V – Coreless constructions using layer pairs.
- Type VI – Alternate constructions in which electrical interconnections and mechanical structure are formed simultaneously.

1.2.4 Printed Circuit Board Assembly Types A type designation signifies further sophistication describing whether components are mounted on one or both sides of the packaging and interconnecting structure. Type 1 (Figure 1-1) defines an assembly that has components mounted on only one side; Type 2 (Figure 1-2) is an assembly with components on both sides.

The need to apply certain design concepts should depend on the complexity and precision required to produce a particular land pattern or printed board structure. Any design class may be applied to any of the end-product equipment categories. Therefore, a moderate complexity (Type 1B) would define components mounted on one side (all surface mounted) and, when used in a Class 2 product (dedicated service electronics), is referred to as type 1B, Class 2. The product described as Type 1B, Class 2 might be used in any of the end-use applications with the selection of class being dependent on the requirements of the customers using the application. See Table 1-1 for description of various board and assembly types.

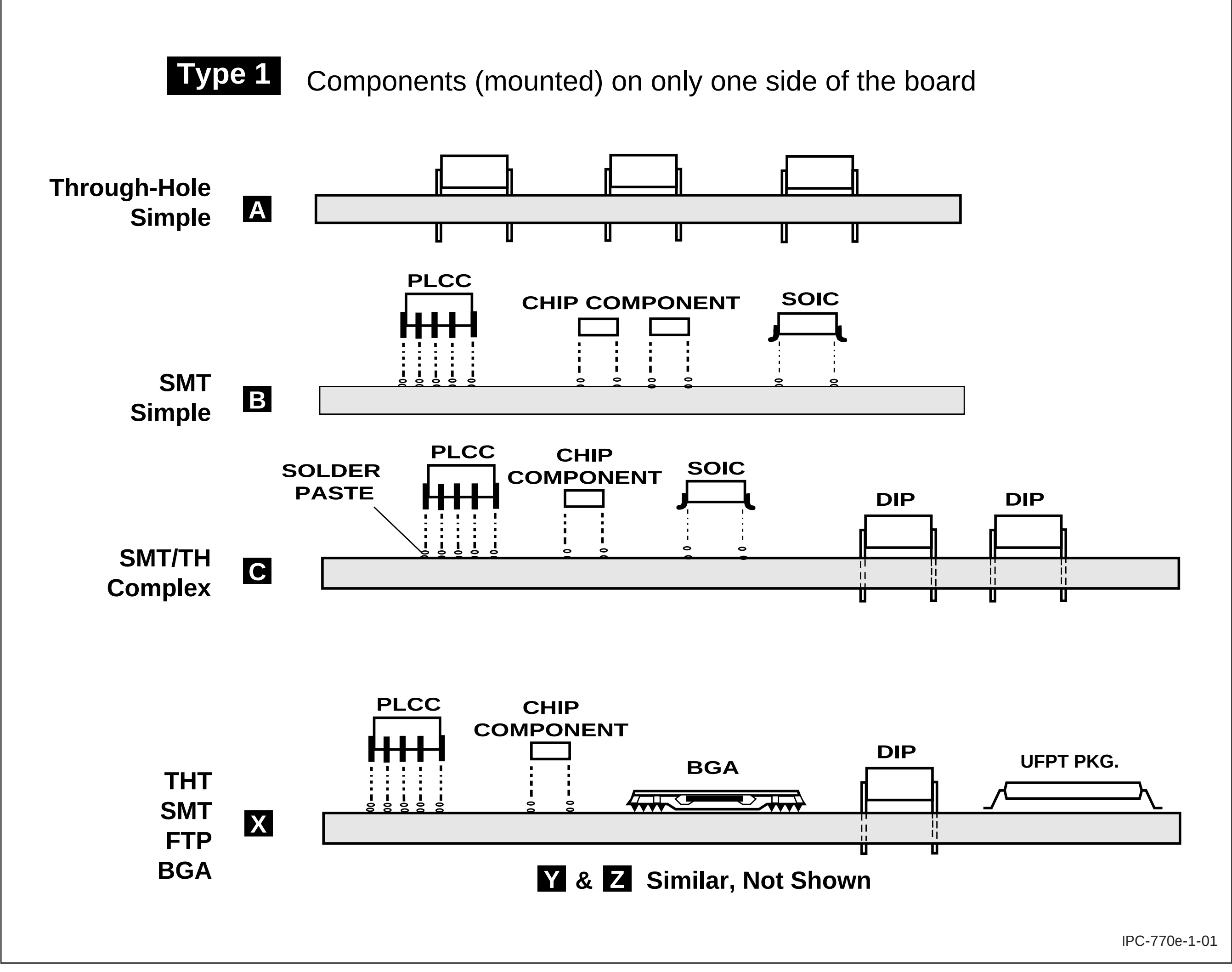


Figure 1-1 Type 1 Printed Board Assembly

1.3 Order of Precedence In the event of any conflict in the development of new designs, the following order of precedence shall prevail:

1. The procurement contract.
2. The approved master drawing or assembly drawing (supplemented by an approved deviation list, if applicable).
3. This standard.
4. Other applicable documents.

1.4 Presentation All dimensions, tolerances and other forms of measurement (temperature, weight, etc.) in this standard are expressed in SI (System International) units with Imperial English equivalent dimensions provided in brackets. Dimensions and tolerances use millimeters as the main form of dimensional expression; micrometers are used when the precision required makes millimeters too cumbersome. Celsius is used to express temperature. Weight is expressed in grams. Users are cautioned to employ a single dimensioning system, and not intermix millimeters and inches. Reference information is shown in parentheses.

1.5 Terms and Definitions The definition of all terms used herein shall be as specified in IPC-T-50 (those terms denoted with an asterisk are cited directly from IPC-T-50), or as listed below:

Anisotropic Conductive Contact – An electrical connection using an anisotropic conductive film or paste wherein conductive particles of gold, silver, nickel, solder, etc., are dispersed. When it is compressed, an electrical connection is attained only in the direction of compression.

Application Specific Integrated Circuit (ASIC) – A semiconductor device intended to satisfy a unique circuit function.

Axial Lead – Lead wire extending from a component or module body along its longitudinal axis.

Ball Lift – A category of ball bond failure in which the ball lifts from the surface of the integrated circuit die bond pad

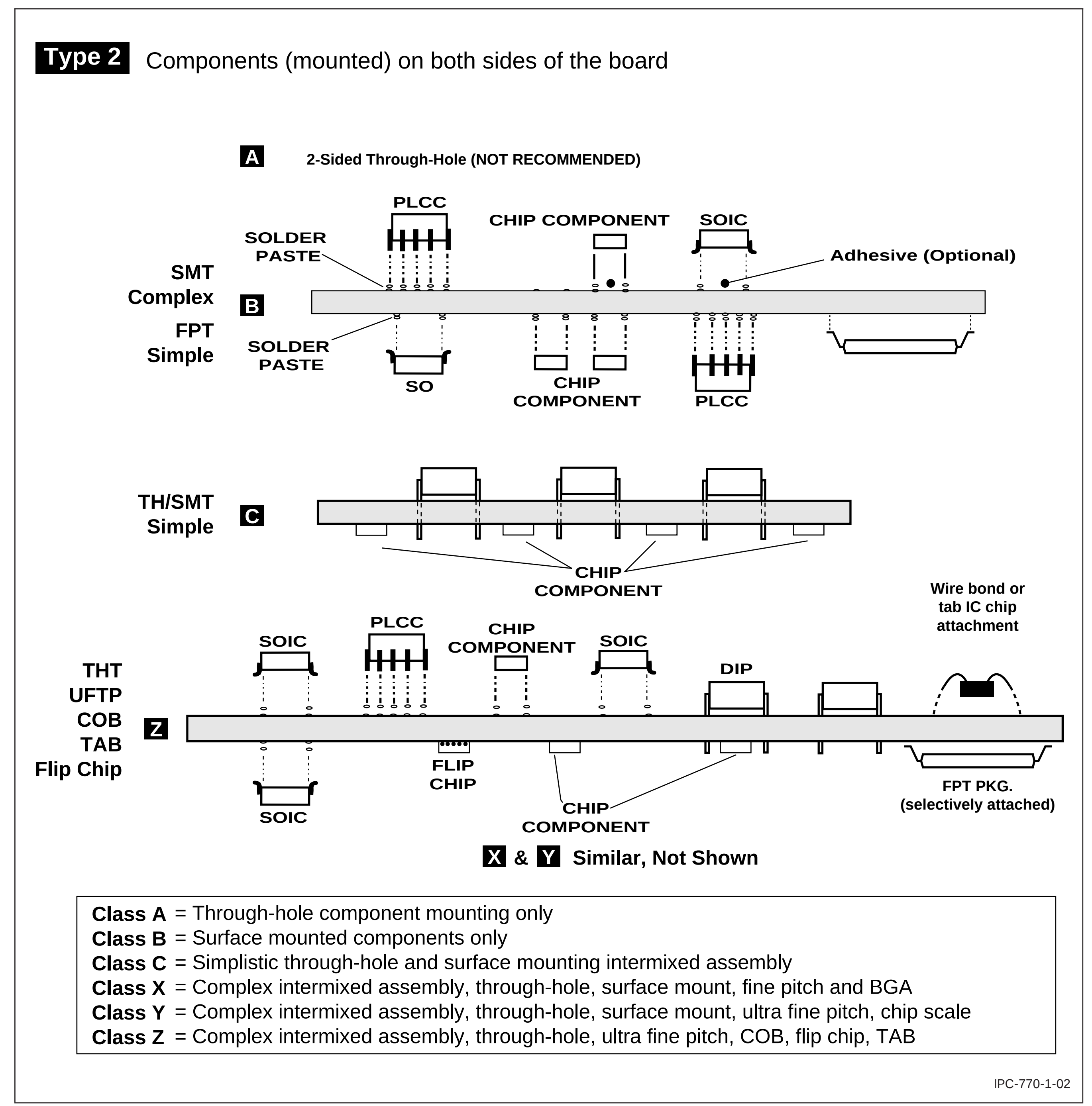


Figure 1-2 Type 2 Printed Board Assemblies

metallization or lifts the metallization from the surface of the underlying oxide or silicon.

Ball Grid Array (BGA) – A surface mount package wherein the bumps for terminations are formed in a grid on the bottom of a package.

Ball Bond* – The welded connection of a bond wire to the bond pad of an integrated circuit die. The bond wire is melted to form a ball and the ball is bonded by use of thermo-compression or thermosonic techniques.

Bonding Time (Reflow) – The time duration from the commencement of thermode heatup until the reflow thermo profile is completed.

Castellation – A recessed metallized feature on the edge of a leadless chip carrier that is used to interconnect conducting surfaces or planes within or on the chip carrier.

Ceramic Quad Flat Pack (CQFP) – A Quad Flat Package (QFP) made of a ceramic material hermetically sealed with leads extending from all four sides.

Table 1-1 Interconnection Acronyms and Definitions

PB Printed Board (Bare Board) (All Board Types) The general term for completely processed printed circuit and printed wiring configurations. This includes single-sided, double-sided and multilayer boards made from rigid, flexible, rigid-flex combinations or with high-density microvia dielectric material combinations.		
PCB Printed Circuit Board Rigid, Flex, PC Card A printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base.	**PWB Printed Wiring Board Rigid, Flex, PC Card** A printed board that provides point-to-point connections, but not printed components in a predetermined arrangement on a common base.	**HDB High Density Board Single/ Multichip, High Density** A printed board that consists of microvias and fine-line point-to-point interconnections, in a predetermined arrangement, on a common passive or active PCB/PWB core.
PCA Printed Circuit Assembly An assembly that uses a printed circuit board for component mounting and interconnecting purpose.	**PWA Printed Wiring Assembly** An assembly that uses a printed wiring board for component mounting and interconnecting purposes.	**HDA High Density Assembly** An assembly that uses a high density board for component or microcircuit (bare die) mounting and interconnecting purposes.
HDCB High Density Circuit Board A printed circuit board core that provides microvia connections and fine-line point-to-point connections, in a predetermined arrangement on one or both sides of the printed circuit board core.	**HDWB High Density Wiring Board** A printed wiring board core that provides microvia connections and fine-line point-to-point connections, in a predetermined arrangement on one or both sides of the printed wiring board core.	**HDMB High Density Microcircuit Board** A high density circuit or wiring board intended to be used as the mounting substrate inside an electronic component, to become the redistribution layer from one or more bare die to the component package I/Os.
HDCA High Density Circuit Assembly An assembly that uses a high density circuit board for prefabricated and embedded or printed electronic component mounting and interconnecting purposes.	**HDWA High Density Wiring Assembly** Density wiring board for prefabricated electronic component mounting and interconnecting purposes.	**HDMA High Density Microcircuit Assembly (Single Chip Module)** An assembly that uses a high density microcircuit board as the redistribution layer for bare die/dice mounting and interconnecting purposes.

Ceramic Pin Grid Array (CPGA) – A pin grid array package (PGA) made of a ceramic material, hermetically sealed by metal, with leads formed on a grid extending from the bottom of the package.

Ceramic Dual-Inline-Package (CERDIP) – A dual-inline-package that has a package body of ceramic material and hermetically sealed by a glass; (see also ''Dual-Inline-Package'').

Chip Carrier – A low profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package. (It can be leaded or leadless.)

Chip Component – A component designed for surface mounting with two or more terminations, attachable with solder or electrically conductive adhesive.

Chip-In-Board (CIB) – An electronic component chip is inserted into an opening of a ceramic or glass-epoxy substrate and bonded by wire bonding or TAB techniques. The object of this technique is to reduce the thickness of the Chip-On-Board assembly. A resin may cover the chip after bonding.

Chip-On-Board Assembly – A printed board assembly using a combination of uncased chips and other devices. The silicon area density is less than 30%.

Chip-On-Flex (COF) – Surface mounted chip attached directly onto flexible printed boards.

Chip-On-Glass (COG) – An assembly technology that uses an unpackaged semiconductor die mounted directly on a glass substrate such as a glass plate for liquid crystal display (LCD).

Clinched Lead – A component lead that is inserted through a hole in a printed board and is then formed in order to retain the component in place to make metal-to-metal contact with a land prior to soldering. See also ''Partially-Clinched Lead.''

Clinched-Wire Through Connection – A connection made by a bare wire that has been passed through a hole in a printed board and subsequently formed (clinched) and soldered to the conductive pattern on each side of the board (see Figure 1-3).

Coined Lead – The end of a round lead that has been formed to have parallel surfaces that approximate the shape of a ribbon lead.

Conductive Paste – A conductive material used for thick film circuits that is a creamy mixture of metal powders and a vehicle material. A conductor is produced by screen printing the paste on a base material and then firing or curing.

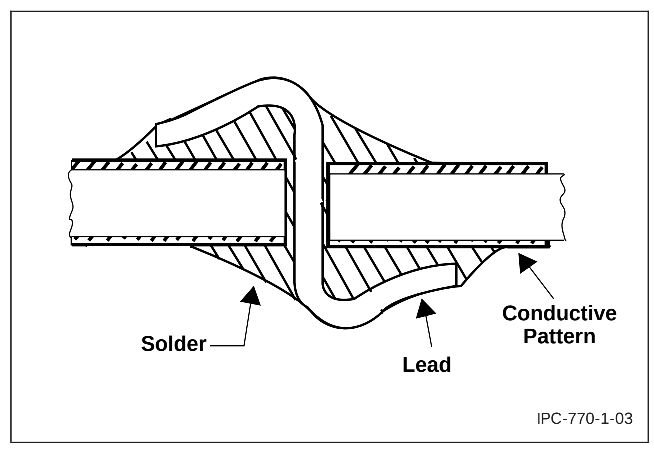


Figure 1-3 Clinched Wire Through Connection

***Conductive Pattern* –** The configuration or design of the conductive material on a base material. (This includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the printed board manufacturing process.)

***Controlled Collapse Bonding (CCB)* –** A bonding technique that makes termination by reflowing the solder bump on a chip and connecting it to the land on the printed board.

***Controlled Collapse Soldering** –** A technique for soldering a component (i.e., flip chip, chip scale package, BGA) to a substrate, where the component connection surface tension forces of the liquid solder supports the weight of the component and controls the height of the joint.

***Component Lead* –** The solid or stranded wire or formed conductor that extends from a component to serve as a mechanical or electrical connector, or both.

***Component Pin* –** A component lead that is not readily formable without being damaged.

***Coplanarity* –** The distance in height between the lowest and highest leads, terminations or bumps when the component is in its seating plane.

***Design for Reliability (DfR)* –** Design procedure to assure long-term reliability of electronic assembly.

***Die* –** The uncased and normally leadless form of an electronic component that is active or passive, discrete or integrated.

***Die Pad* –** A land on which the integrated circuit die is mounted during the assembly process using adhesives.

***Dual-Inline Package (DIP)* –** A basically-rectangular component package that has a row of leads extending from each of the longer side of its body that are formed at right angles to a plane that is parallel to the base of its body.

***Eyelet* –** A short metallic tube, the ends of which can be formed outward in order to fasten it within a hole in material such as a printed board.

***Face Down Bonding* –** A type of integrated circuit bonding wherein the die circuitry faces the substrate or the lead frame.

***Face Up Bonding* –** A type of integrated circuit bonding wherein the back of the die is attached to a base material.

***Fine Pitch QFP* –** A quad flat pack package with the lead pitch less than 0.625 mm.

***Fisheye (Prepreg)** –** A localized area of the reinforcement where the resin coverage is significantly diminished although intact, forming a circular depression, much like a hollow volcano.

***Flat Pack* –** A rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body.

***Gull Wing Leads* –** An SMT lead form. Leads extending horizontally from the component body centerline, bent downward immediately past the body and then bent outward just below the bottom of the body, thus forming the shape of a gull's wing.

***Heat Absorption Coefficient* –** The degree to which various materials absorb heat or radiant energy.

***Humidity Aging* –** The exposure to a humid environment as a preconditioning before testing components, printed boards, or assemblies.

***Inner Layer* –** See ''Internal Layer.''

***J-Leads* –** The preferred surface mount lead form used on PLCCs, so named because the lead departs the package body near its Z axis centerline, is formed down then rolled under the package. Leads so formed are shaped like the letter ''J.''

***Land* –** A portion of a conductive pattern usually, but not exclusively, used for the connection and/or attachment of components.

***Land Pattern* –** A combination of lands that is used for the mounting, interconnection and testing of a particular component.

***Land Grid Array (LGA)* –** A square or rectangular package with termination lands located in a grid pattern on the bottom of the package.

***Large-Scale Integrated Circuit (LSI)* –** An integrated circuit with over 100 gates.

Lead Extension – Part of a lead or wire that extends beyond a solder connection.

Lead Frame* – The metal frame on which the integrated circuit die is mounted and bonded during the assembly process.

Lead Fingers – The interior ends of the lead frame leads to which the bond wires from the integrated circuit are connected.

Leadless Chip Carrier (LCC) – A chip carrier whose external connections consist of leads that are around and down the side of the package; (see also ''Leadless Device'').

Leadless Device – See ''Die'' and ''Leadless Surface Mount Component.''

Leadless Surface-Mount Component – A surface-mount component whose external connections consist of metallized terminations that are an integral part of the component body; (see also ''Leaded Surface-Mount Component'').

Leaded Surface-Mount Component – A surface-mount component for which external connections consist of leads that are around and down the side of the package; (see also ''Leadless Surface-Mount Component'').

Least Material Condition (LMC) – The condition in which a feature of size contains the least amount of material within the stated limits of size.

Locating Accuracy – The accuracy in the positioning of a component described by the amount of displacement (i.e., diameter of true position) from the desired position.

Manufacturing Exposure Time (Component) – The time after bake that the component manufacturer requires to process the components prior to bag seal, including a default amount of time to account for shipping and handling.

Maximum Material Condition (MMC) – A drawing defining certain characteristics of the printed board, such material within the stated limits of size.

Metal Electrode Face (MELF) – MELF leadless components have metallized terminals at both ends of a cylindrical body.

Migration (Pressure Sensitive Tape) – The movement over a long period of time of an ingredient from one component to another when the two are in surface contact. May occur between tape components or between the tape and the surface to which it is applied.

Mixed Component Mounting Technology – A component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure.

Molded Interconnection Device (MID) – A combination of molded plastic substrate and conductive patterns that provides both the mechanical and electrical functions of an electronic interconnection package.

Mounting Tack Time – The interval of time required for mounting one component or all components in the solder paste on a printed board.

Multichip Module (MCM)* – A multichip module consisting primarily of closely-spaced integrated circuit dice that have a silicon area density of 30% or more.

Multichip Module-Ceramic (MCM-C) – Multichip modules where the materials of the mounting structure are ceramic or glass-ceramic alternatives; (see also ''Multichip Module'').

Multichip Module-Deposited (MCM-D) – Multichip modules where unreinforced dielectric and conductive materials are added sequentially to form an interconnect structure on a substrate; (see also ''Multichip Module'').

Multichip Module-Laminate (MCM-L) – Multichip modules primarily using printed board manufacturing processes and materials; (see also ''Multichip Module'').

Package Cracking – Cracks in a plastic integrated circuit package caused by stress that results from exposure to reflow solder temperature. These cracks may propagate from the die or die pad to the surface of the package, or only extend part way to the surface or lead fingers.

Planar Resistor – An etched or deposited resistive element incorporated within or on the surface of the printed board.

Plastic Ball Grid Array (PBGA) – A polymer based package with interconnects formed of tin-lead solder spheres. The solder interconnects are located in an array area on the bottom side of package.

Plastic Leaded Chip Carrier (PLCC) – A surface mount family of integrated circuit packages with J-leads extending from all four sides of the package, generally with a 1.27 mm lead-to-lead pitch.

Plastic Quad Flat Pack (PQFP) – A surface mount family of integrated circuit packages with leads exiting from all four sides of the package and formed into ''gull-wing'' lead format.

Polarized Component – A component wherein the terminations are assigned as positive or negative electrical polarity.

***Quad Flat Pack (QFP)* –** A square component package with leads that are formed in ‘‘gull-wing’’ shape and extend from the four sides of the body.

***Quad Flat Pack With Bumpers (BQFP)* –** A QFP package with guarding bumpers at the four corners to protect the leads from damage.

***Radial Lead Component* –** A component where the leads are located on the bottom, radially and parallel to the central axis.

***Radial Lead* –** Lead wire extending from the axis of a component or module body at the mounting surface.

***Rectangular Lead* –** A lead form or leg shape whose cross-section is rectangular in shape.

***Reflow* –** The joining of surfaces that have been tinned and/or have solder between them, placing them together, heating them until the solder flows, and allowing the surface and the solder to cool in the joined position.

***Seating Plane* –** The surface of a substrate on which a component rests.

***Self-Alignment Effect* –** A force that pulls an SMD to the center of the land by the surface tension of the solder during reflow soldering.

***Shrink Sop (SSOP)* –** A family of component packages with four sizes, each having the ability to provide lead pitches between 0.68 mm and 0.3 mm.

***Single Chip Package (SCP)* –** An integrated circuit package containing only one semiconductor die.

***Single In-Line Package (SIP)** –** A component package that terminates in one straight row of pins or leads.

***Small Outline (SO)* –** See page 46 of DRM-18F for definition.

***Small Outline I-Leaded Package (SOI)* –** A component package of SOP type with the leads shaped like the letter ‘‘I.’’

***Small Outline Integrated Circuit (SOIC)* –** A surface mount family of integrated circuit packages with two rows of formed leads with 1.27 mm pitch (center-to-center spacing). Lead formation may be ‘‘J’’ or ‘‘gull wing.’’

***Small Outline J-Leaded Package (SOJ)* –** Small outline package (SOP) with J-leads.

***Small Outline Package (SOP)* –** An integrated circuit package with leads of ‘‘gull wing’’ shape extending from two sides of its body.

***Small Outline Transistors (SOT)* –** SOTs are rectangular transistor or diode packages with three or more gull-wing leads.

***Surface Mounting** –** The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

***Surface Mount Component* –** A leaded or leadless device (part) that is capable of being attached to a printed board by surface mounting.

***Surface Mount Device* –** See ‘‘Surface Mount Component (SMC).’’

***Thin Quad Flat Pack (TQFP)* –** A surface mount family of integrated circuit packages with a thin plastic body.

***Thin Small Outline Package (TSOP)* –** A package that has the same features as the Small Outline Package except that its thickness is reduced to 0.8 mm - 1.2 mm.

***Through-hole Mounting* –** The electrical connection of components to a conductive pattern by the use of component holes.

***Transistor Outline (TO)* –** JEDEC Designation for Transistor Packaging Outline.

***Tray* –** A pallet intended to contain surface mount devices (SMD) designed to make it easy to feed them to an automatic component-mounting machine.

***Through Hole* –** The electrical connection of components to a conductive pattern by the use of component holes.

***Very Large Scale Integrated Circuit (VLSI)* –** Integrated circuits with more than 80,000 transistors on a single die that are interconnected with conductors that are 1 micron or less in width.

***Wire Bond Degradation* –** A weakening of an integrated circuit ball bond due to stress caused by exposure to reflow soldering temperatures resulting in possible reduction of component reliability.

***Zigzag In-Line Package* –** A package with in-line leads on one side that is arranged in zigzag fashion.

2 APPLICABLE DOCUMENTS

There are many other resources to where designers may wish to refer. While some of these may be outdated or even cancelled, there is still good support information found in them.

2.1 IPC[1]

IPC-DRM-18 Component Identification Training & Reference Guide

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-SC-60 Post Solder Solvent Cleaning Handbook

IPC-SA-61 Post Solder Semi-Aqueous Cleaning Handbook

IPC-AC-62 Post Solder Aqueous Cleaning Handbook

IPC-CH-65 Guidelines for Cleaning of Printed Boards

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-325 Documentation Requirements for Printed Boards, Assemblies, and Support Drawings

IPC-D-350 Printed Board Description in Digital Form

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-A-610 Acceptability of Electronic Assemblies

IPC-HDBK-610 Handbook and Guide to IPC-A-610

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-CA-821 General Requirements for Thermally Conductive Adhesives

IPC-CC-830 Electrical Insulating Compounds for Printed Board Assemblies

IPC-HDBK-830 Guidelines for Design, Selection and Application of Conformal Coatings

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-1902 IPC/IEC Grid Systems for Printed Circuits

IPC-2221 Generic Standard for Printed Board Design

IPC-2222 Sectional Standard on Rigid PWB Design

IPC-2223 Sectional Design Standard for Flexible Printed Boards and Assemblies

IPC-2224 Sectional Standard for Design of PWBs for PC Cards

IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

IPC-2226 Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-3406 Guidelines for Electrically Conductive Surface Mount Adhesives

IPC-3408 General Requirements for Anisotropically Conductive Adhesives Films

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6013 Specification for Printed Wiring, Flexible and Rigid-Flex

IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-7095 Design and Assembly Process Implementation for BGAs

IPC-9501 PWB Assembly Process Simulation for Evaluation of Electronic Components (Preconditioning IC Components)

IPC-9502 PWB Assembly Soldering Process Guideline for Electronic Components

IPC-9503 Moisture Sensitivity Classification for Non-IC Components

IPC-9504 Assembly Process Simulation for Evaluation of Non-IC Components (Preconditioning Non-IC Components)

1. www.ipc.org

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

2.2 Joint Industry Standards[2]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC-HDBK-001 Handbook and Guide to Supplement J-STD-001

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

J-STD-004 Requirements for Electronic Soldering Fluxes

J-STD-005 Requirements and Test Methods for Solder Paste

J-STD-006 General Requirements and Test Methods for Electronic Grade, Soft Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-012 Implementation of Flip Chip and Chip Scale Technology

J-STD-020 Handling requirements for Moisture Sensitive Components

J-STD-026 Semiconductor Design Standard For Flip Chip Applications

J-STD-033 Standard for Handling, Packaging, Shipping and Use of Moisture Reflow Sensitive Surface Mount Devices

J-STD-035 Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components

2.3 Electronic Industries Association[3]

RS-471 Symbol and Label for Electrostatic Sensitive Devices

2.4 EOS/ESD Association Documents[4]

ANSI/ESD-S8.1 ESD Awareness Symbols

ANSI/ESD-S-20.20 Protection of Electrical and Electronic Parts, Assemblies and Equipment

2.5 JEDEC[5]

Publication 95 Mechanical Outlines of Solid State and Related Products

Publication 95-1 Design Requirements for BGA and FBGA

3 GENERAL GUIDELINES

The component mounting technique, the mounting sequence and the resultant assembly configuration all impact the soldering techniques that can be applied to the interconnection of components, printed boards and the resultant quality of the solder joints.

Excessively large clearances can result in draining of the solder. Lead extension through the hole must be adequate to ensure opportunity for a good solder joint and subsequent inspection but not so long as to cause interference with tooling for subsequent processes or shorting to adjacent runs or assemblies.

Component and board considerations, independent of type that impact soldering should be considered.

3.1 Design Options and Considerations When first considering assembly options some basic decisions have to be made. Decisions such as whether to use solder or adhesives for component attachments, whether to surface mount, through board mount or use a mixture of both, whether even newer techniques such as chip-on-board should be considered. Selections of placement methods and equipment and choices of solder material form lead to questions about material application methods and equipment.

The type of component used is normally dependent on the type of assembly. For example, single-sided assemblies often use through-hole components only, whereas double sided/multilayer assemblies often use surface mounted or intermixed components. In the former case, the through-hole components are frequently wave soldered. In the latter case, the surface-mounted components may be reflow soldered, or those surface-mounted components on the underside of the board may be attached with adhesives and then wave soldered.

If the printed board structure is complicated, or only a small number of assemblies are to be made, then manual assembly techniques are often used. However, if the printed

2. www.ipc.org
3. www.eia.org
4. ESD Association, 7900 Turin Road, Bldg. 3, Ste. 2, Rome, NY 13440
5. www.jedec.org

board structure is simple, or the number of assemblies required is large, then the set-up time and monetary investment for automated component mounting and assembly may be worthwhile.

In either case, component mounting on double sided or multilayer printed boards is more complicated than single-sided boards because the former use plated-through holes for the through-board components. These plated-through holes require greater tolerances because plating builds up in the holes. This may restrict component mounting.

The joining techniques used may also influence the assembly process. Although this document deals primarily with component mounting, not the joining process, the two cannot be separated in intermixed assemblies. In some sequential manufacturing operations, certain parts must be secured or permanently attached before other components are mounted.

The assembly process itself often influences component placement. For example, singular (one at a time) or multiple (several at a time) component placement affects toolhead clearances for automatic placement equipment, set up procedures, and other manufacturing steps.

The entire sequence of events in the assembly/joining process affects component placement. Previously mounted components must not interfere with other components mounted in a second step and secondary-joining techniques, such as soldering, must not damage components previously placed and joined.

In some cases, simply selecting a different assembly/joining procedure cannot solve problems in assembly. Perhaps the problem cannot be ‘‘solved’’ at all, but it can be prevented through careful design. To prevent problems and create a board that can be manufactured, the designers of printed board assemblies must take into account all of the fabrication assembly steps necessary to complete the electronic assembly.

3.1.1 Leadless Component Terminations This geometry provides no compliance and results in a very rigid, small lap solder joint depending on the reflowed solder material system providing desired mechanical properties. Visual inspection of the joint is limited to fillet appearance on any castellation and pad extension. Cleaning is more difficult with this geometry than with the leaded termination.

3.1.1.1 Lead/Land Relationships The leadless and leaded terminations provide different solder joint geometries and the stress distribution is different in each case. If leads are too short to protrude through the printed board or if the surface mount lands are too small, soldering may become difficult. Printed board hole diameters must be considered for the type product to be used.

Costs and problems can be reduced if the designer selects his devices prior to printed board design and then designs the proper hole or land size, etc. ‘‘Nonstandard’’ holes and land patterns increase costs by making ‘‘nonstandard’’ devices mandatory.

3.1.2 Leaded Component Terminations This geometry results in a narrow solder fillet. It provides compliance that can compensate for some degree of mismatch in expansion between the component package and the substrate. Visual inspection of solder joints is somewhat easier with this geometry. Cleaning operations are aided by this geometry since it provides clearance between the bottom of the component and the substrate. Excess solder fillets on this geometry can stiffen the lead and reduce any compliance advantage.

3.1.2.1 Lead/Hole Relationships Hole and land requirements for intermixed assembly are identical to those requirements in through hole and surface mounted land pattern configurations. No special requirements are necessary and implementation of the proper land pattern into the design provides the appropriate solder joint after placement.

3.1.3 Spacing Proper spacing can greatly increase automatic, semiautomatic and manual speed of component placement. If possible, features should be placed in straight-line patterns rather than random ones. They should also be placed so that readjustment of the board to the product is unnecessary. Additional considerations:

- Tooling holes should be placed as far apart as possible.
- No premounted components should interfere with the proper machine installation of those devices to be subsequently installed.
- Printed board holes may be ‘‘non’’ plated or ‘‘through’’ plated, drilled or punched, depending on the device that is eventually used and the quality required in the final printed board.

As a general rule, a drilled hole is more consistent in size and is advised where a hole will eventually be plated through. Punched holes in multilayer printed boards are not recommended since the internal conductors may be damaged.

3.1.4 Part Type Mass soldering of assemblies is usually done with either a solder wave or a reflow process with hot air, radiation (infrared), condensation heat transfer or conductive plate. Many leaded devices such as chip carriers

are currently not considered appropriate for wave soldering and must be soldered with the reflow process. These devices may appear on either side of the board. However, if processing includes a wave-solder operation, SMT components on the solder destination side should be reflowed. Surface mounted devices with fewer leads such as resistors, capacitors and small outline (SO) devices can be assembled with solder waves but the orientation of the parts becomes important. Passive chips, SOTs, SOICs and other components that can tolerate immersion in the molten solder of a wave soldering machine may be mounted on the ''solder source'' side of printed wiring assemblies.

Through-hole mounted parts have the potential of resultant lower quality solder joints if insulation material, potting compound or other material is allowed to protrude into the hole. Another characteristic of these devices is their tendency to ''rise'' during the fluxing/wave soldering process if not clinched or mechanically retained. For wave soldering, the through hole mounted devices should be mounted on the ''solder destination'' side of the board. These devices may not be compatible with reflow processes. The component mass is another factor to be reviewed. Heavy mass components require longer soldering times due to their heat sinking characteristics.

3.2 Assembly Considerations

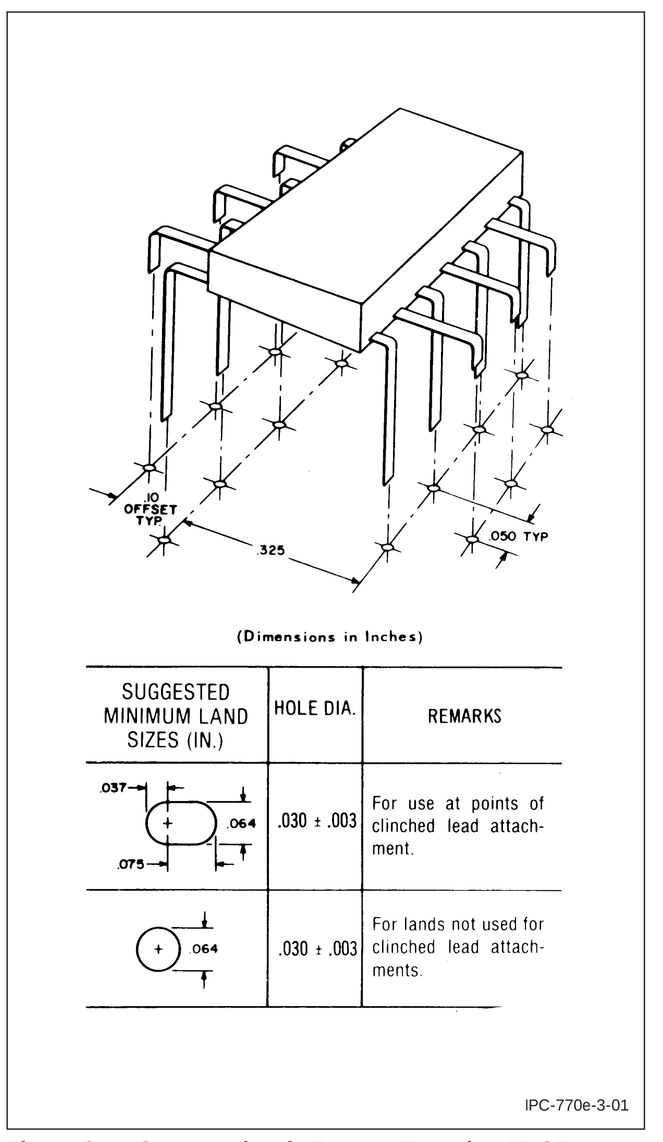
3.2.1 Component Preparation All lead extension and forming requirements for parts to be mounted on printed board structures are identical to the techniques described for through hole and surface mount component mounting and positioning.

Sometimes it is necessary to modify a component so that it can be mounted in a different manner. For example, forming the leads of a through-hole component so that it could be surface mounted. This could result in the elimination of a wave soldering process.

Figure 3-1 shows taking a standard flatpack that is usually surface mounted and forming the leads to mount the component in the through hole. This practice would be used when only several flatpacks are present on an otherwise all through-mounted board assembly.

Sockets are sometimes used so surface mount components may be placed in through-hole assemblies.

When components designed for through hole are converted to surface mount, there are additional steps necessary in lead forming. Axial leaded parts that are normally mounted through hole would have their leads coined as shown in Figure 3-2. These parts could then be surface mounted. In addition, some manufacturers have started to use the concept of a dual-in-line package (DIP) with I beam leads. In



SUGGESTED MINIMUM LAND SIZES (IN.)	HOLE DIA.	REMARKS
.037 × .075, .064 (oblong land)	.030 ± .003	For use at points of clinched lead attachment.
.064 (round land)	.030 ± .003	For lands not used for clinched lead attachments.

Figure 3-1 Staggered Hole Pattern Mounting "MO" Flatpack Outline Drawing (Only Inches Shown)

this technique, the DIPs have their leads trimmed and are surface mounted to the board in the manner shown in Figure 3-3. Special care must be taken to insure that the components do not move during the soldering operations. Usually the solder paste is sufficient to hold a dual inline package in place prior to reflow soldering. This method is not acceptable for Class 3 assemblies.

3.2.2 Lead Forming When component leads require forming, the leads should be formed with a bending tool. The component leads should be formed to the final configuration before assembly or installation (except for the final crimp, where required). When being bent, a suitable tool should firmly hold the welded leads on the side of the weld away from the component body. Lead forming should not nick the lead. Care must be taken so that energy (mechanical shock) from the bending action is not transmitted into the component.

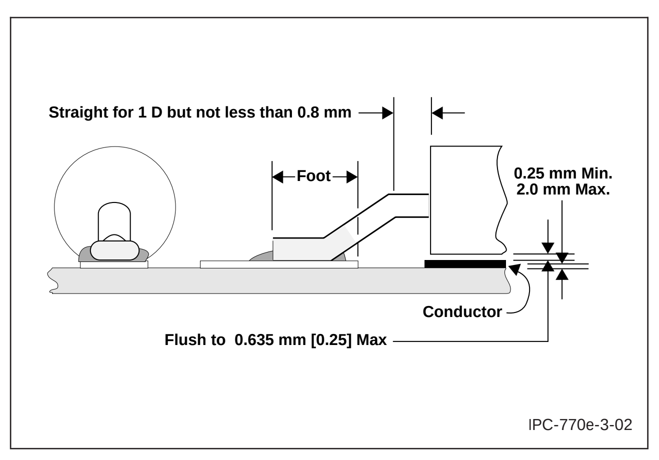


Figure 3-2 Component Modifications for Surface Mounting Applications

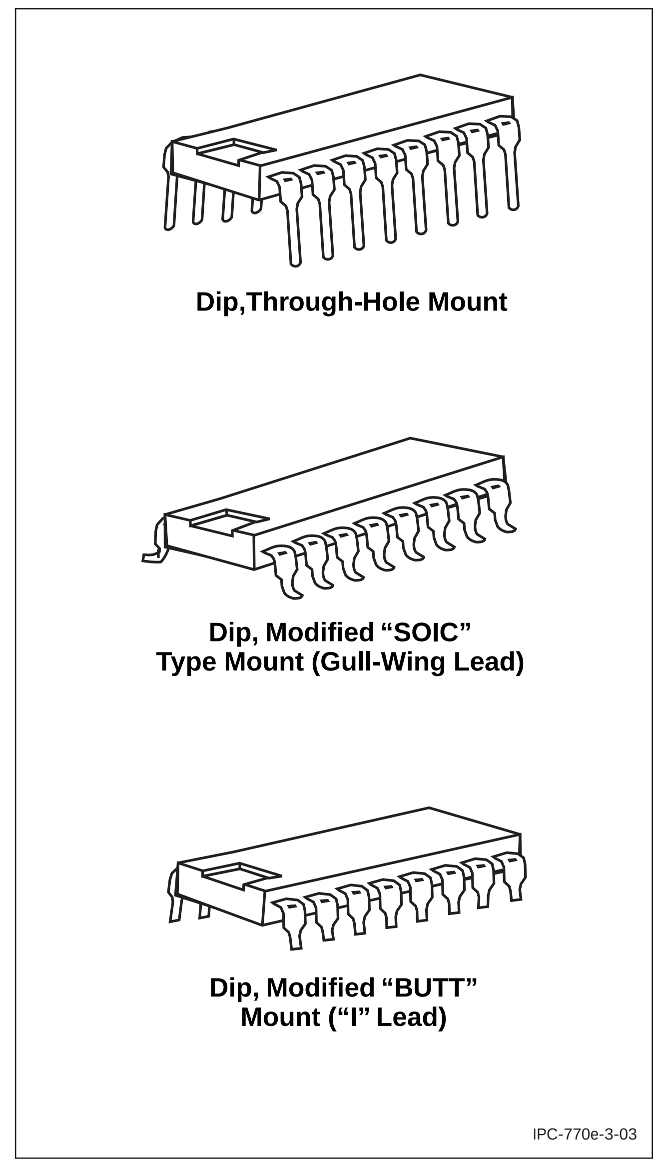


Figure 3-3 Modifying DIP for Surface Mounting

Lead forming tools and forming tolerances have significant impact on maintaining functional quality of components. Considerations must be given to lead material and hardness when designing tooling. Component body materials (glass, elastomers, metal case, plastic) react differently to forming strains. Stresses from gripping and close bending may damage protective cases.

Nicks, cuts or other cross-section reduction to leads during the gripping and forming process can provide failure mechanisms and change electrical characteristics. Care should be exercised in tool design and materials. Following specific guidelines on closeness of bend and minimum bend radii is necessary.

3.2.3 Component Placement Sophisticated tooling is available, both for the placement of axial leaded components and the placement of surface mounted components. Figure 3-4 shows an example of the sequencing used for placing two leaded axial parts and a tape used to place chip components between the parts. Also, machine head clearances must be considered.

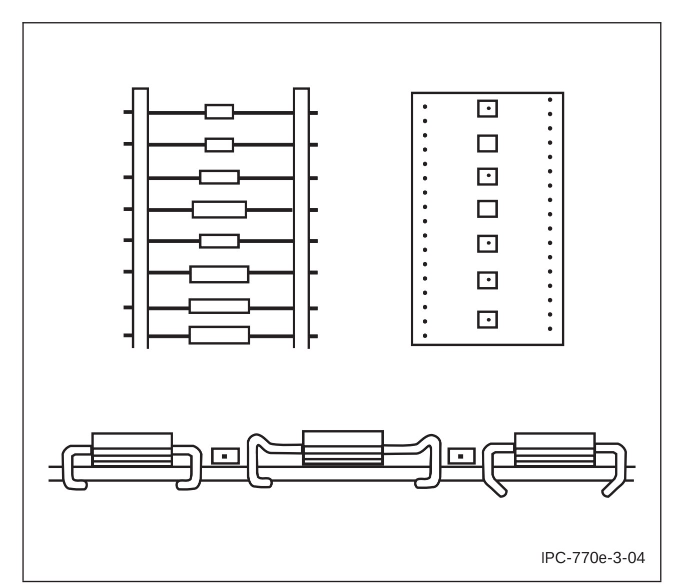
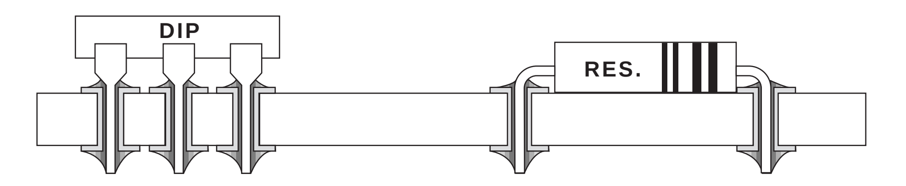


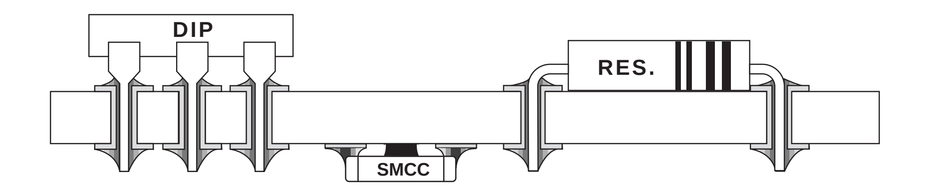
Figure 3-4 Placement Machine Considerations

In the example shown, the chip resistors would be placed first and probably attached through reflow soldering. The design must provide adequate clearances for the machine that assembles and clinches the leads for the axial leaded components. Without proper knowledge of machine clearances or considerations included into the design, manufacturers would have to insert components semiautomatically or use manual techniques.

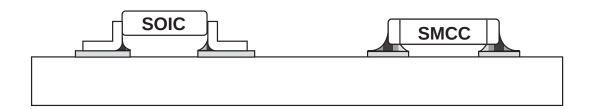
3.2.4 Mixed Assemblies In the example shown in Figure 3-5, the chip resistors would be placed first and probably attached through reflow soldering. The design must provide an adequate clearance for the machine.



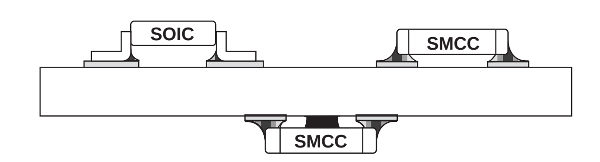
Type 1A Simple Through-Hole



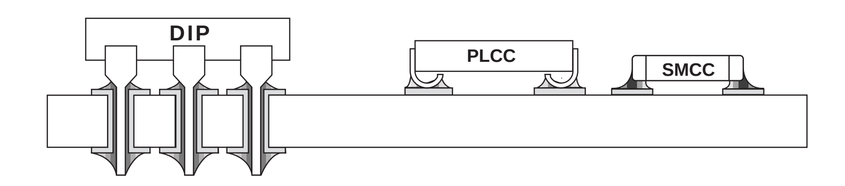
Type 2C Simple Mixed Through-Hole & Surface Mount



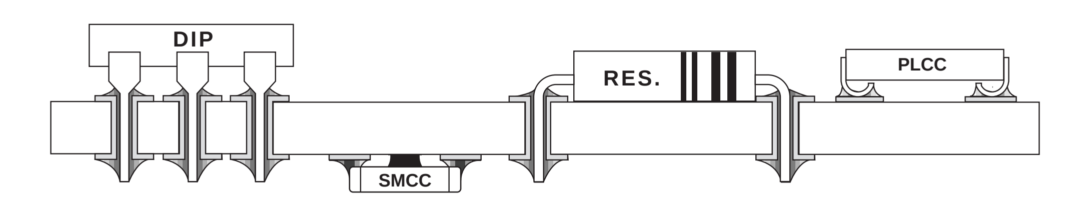
Type 1B Simple One Side Surface Mount



Type 2B Simple Surface Mount on Two Sides



Type 1C Simple Mixed Through-Hole & Surface Mount on One Side



Type 1A Simple Mixed Through-Hole & Surface Mount on Two Sides

IPC-770e-3-05

Figure 3-5 Mixed Assemblies

3.2.5 Component Securing Forming of leads for through-hole mounting components serves many purposes. These include retaining the component in the substrate during subsequent handling prior to soldering or providing a standoff. Such bends or loops are provided by tooling with some forming machines and/or can be introduced by hand forming. Care must be exercised such that stresses are not introduced to the component, leads or solder joint during solidification.

The shock and vibration to which printed board components are subjected during normal handling, environmental testing and use can damage the lead terminations and lead-to-component body seals. For this reason, many components should be mechanically secured to the mounting base.

The component securing methods most commonly used are clips, clamps, and brackets, wire and elastic straps, adhesives and integral mounting provisions.

Most circuit malfunctions in a severe vibration environment are caused by cracked solder attachments, cracked seals, or broken electrical lead wires. These failures are usually due to dynamic stresses that develop because of relative motion between the electronic components and the board. This relative motion is generally most severe during resonant conditions.

Since shock and vibration vary widely with each specific application, it is not possible to provide solutions to all component-mounting problems. This document suggests some general guidelines that, if observed, provide reasonable assurance that the components and assemblies survive shock and vibration within their intended use.

The extent to which the user wishes to implement these guidelines may ultimately be validated by actual tests of the assembled printed board in its intended shock and vibration environment.

The ultimate ability of components to survive in shock and vibration environments depends upon the degree of consideration given to the following factors:

- Worst case levels of shock and vibration environment for the entire structure in which the printed board assembly resides and the ultimate level of this environment that is actually transmitted to the components mounted on the board. Particular attention should be given to equipment that is subjected to random vibration.
- Method of mounting the board in the equipment to reduce the effects of this environment, specifically the number of board-mounting supports and their interval and complexity.
- Attention given to the mechanical design of the board; specifically its size, shape, type of material, material thickness and degree of resistance to bowing and flexing.
- Shape, mass, and location of the components mounted on the board.
- Component lead wire strain relief design as provided by its package, lead spacing, lead bending, or a combination of these with the addition of restraining devices.
- The attention paid to workmanship during board assembly to ensure that component leads are properly bent, not nicked.
- Components are installed in a manner that minimizes component movement.

Techniques for shock and vibration mounting of intermixed assemblies do not vary dramatically from techniques previously described for boards that have only through hole components or are all surface mounted.

One aspect of the intermixed assembly is that although components can take the shock of the final assembly, certain components and their joints may not take the shock of a secondary assembly operation. For example, if chip components are mounted on the underside of the board and attached using some form of adhesive, the next assembly operation should not impart additional shocks to the assembly so that the parts that have been secured to the underside are dislodged.

The characteristic of shock from secondary assembly operations is even more important when parts that have previously been mounted are attached using soldering techniques. Now the shock and vibration is not just on the part itself, shock and vibration can also affect the reliability of the soldered joint.

Special fixturing should normally be provided during the assembly operation to insure that no damage is imparted to those parts that have been previously mounted or attached.

3.2.5.1 Clips, Clamps and Brackets The following list describes the basic guidelines for components mechanically secured by clips, clamps and brackets (see Figure 3-6):

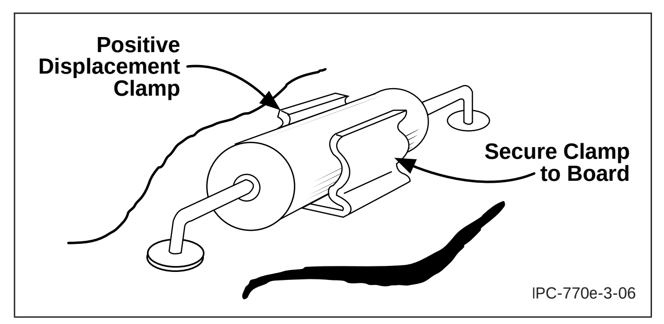


Figure 3-6 Clip-Mounted Component

- All clips, clamps or brackets should be secured using two fasteners or one fastener and a nonturn device to prevent rotation.
- Clamps and brackets that require their removal in order to replace the component should be secured with a threaded

fastener or other nonpermanent fastener, unless the subassembly in which they are used is considered to be disposable or nonrepairable.

- Spring type clips that need not be removed during component replacement may be secured with permanent type fasteners such as rivets or eyelets.
- Twist-type lugs, ears, or clips with glass envelope components should be avoided.

3.2.5.2 Strapping Devices When using wires and elastic straps for mechanical securing, the strap is wrapped over the component body and passed through holes in the mounting base. When wire is used, it is clinched and soldered in the same manner as component leads to lands. When wire is used with heat sensitive or fragile components, the part of the wire on the component should be covered with a suitable sleeving.

The elastic strap is secured by being stretched to reduce its cross-section below that of the hole, and then returned to its larger-than-hole size by relieving the tension after it has been passed through the hole. The resiliency of the strap holds the component in place (see Figure 3-7).

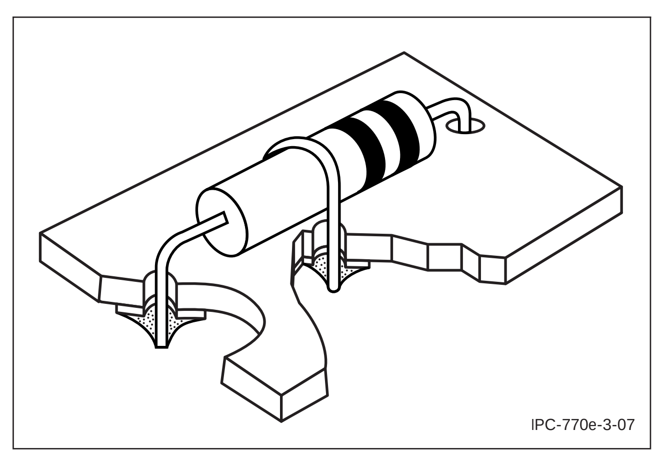


Figure 3-7 Strap Securing

3.2.5.3 Component Securing Devices The shock and vibration to which printed board components are subjected during normal handling and environmental testing can damage the lead terminations and lead-to-component body seals. For this reason, many components, especially those weighing more than 7.09 g per lead, should be mechanically secured to the mounting base prior to lead termination and during assembly usage.

The more commonly used component-securing methods are clips, clamps, and brackets; wire and elastic straps; adhesives and integral mounting provision.

3.3 Materials All soldering processes are only capable of achieving optimum process yields if the materials used in those processes are not substandard. Regardless of the particular soldering process (dip, wave, and reflow), all solder processes follow the same basic steps: flux, preheat and soldering. Some newer technologies use other materials such as adhesives either in conjunction with or in replacement of soldering. Adhesive attachment of components is particularly attractive with temperature sensitive devices, and for securing surface mount devices. The various types of alternative solder materials are discussed here.

3.3.1 Solder Metal alloys with melting points in the range of 150°C to 400°C. Alloys below this temperature range are commonly called fusible alloys while above this range they are called brazes. Tin-lead alloys are most common, although more complex compositions have been developed for special applications.

For electrical soldering, alloys near the eutectic composition (63% tin - 37% lead) have the required combination of properties. Although compositions either side of the eutectic composition have higher liquidus (completely melted) temperatures desirable for higher ambient temperature applications, the initial melting point when solder softens is 183°C; the same for all tin-lead alloys with compositions between 20% and 98% tin. There is no benefit of service temperature unless the tin content is less than 20% or greater than 98%.

The range of properties of tin-lead alloys can be varied by adding other metals such as bismuth or indium to lower the melting point, or antimony, silver, etc., to increase hardness and fatigue resistance. Alloys containing less than 10% tin are used for applications involving temperatures below -40°C. As mentioned earlier, the choice of the soldering flux depends primarily on the solderability of the base material. Solder pastes and alloys should be agreed upon for composition and purity. Solder paste is defined in J-STD-005; solder alloys are defined in J-STD-006.

3.3.2 Flux Must have properties to chemically remove the surface oxide or tarnish and keep the surface clean until the solder has melted and flowed over the fluxed surface.

Soldering fluxes have been divided into three general categories. The traditional flux specifications classify fluxes on the basis of their chemical make-up or flux base (rosin base fluxes, for example, are classified as R, RMA or RA ROLO ROL1 etc.).

J-STD-004 utilizes a unified approach to flux classification based on fundamental, intrinsic corrosive and conductive properties of flux and flux residues, rather than specifying the flux base.

Flux are specified according to one of the following three types of flux/flux residue activity per J-STD-004:

- L = Low (or none)
- M = Moderate
- H = High

Inorganic fluxes are not permitted for electronics soldering.

The flux and the cleaning process (or lack thereof) are directly interdependent.

3.3.2.1 Rosin Flux Many common fluxes use natural rosin as a base. This product, derived from the gum of pine trees, is a mix of abietic acid and numerous dehydrogenation products.

Rosin is a glassy, noncrystalline mixture of organic acids which are inert up to their softening point and only assume an acidic nature when molten. After melting and solidifying, the hard glassy properties render the residue once again inert. Residues from other added chemical activator compounds usually become encapsulated in the rosin residue, which renders them noncorrosive. The effectiveness of this safeguard, however, depends on the quantity and nature of the activator used.

The acidity of pure rosin alone is usually insufficient to clean surfaces to be soldered, so rosin fluxes are usually enhanced by a variety of chemicals called activators. Common activators are inorganic halides, organic halides, carboxylic acids, amines and halogenated amines. The degree of activation achieved by the various chemicals depends upon the compound and the quantity. The overall activity developed is often a synergistic product of more than one activator. Activation is usually quantified not by formulation alone but rather by some secondary property. Examples include the ability of the residue extract to dissolve a copper from the ‘‘Copper Mirror Test’’ or the chemical’s ionic conductivity. The level of activator affects the rate of wetting.

3.3.2.2 Organic Acid (Water Washable) Fluxes These fluxes are significantly more active and aggressive than rosin fluxes in removing oxides from the surfaces to be soldered. They use strong organic acids and salts to achieve these properties. They are more forgiving of poor solderability characteristics of the soldered surfaces.

The increased activity yields flux residues that are more corrosive than the residues of rosin fluxes. Because of their characteristics it is necessary to completely remove the residue with a post soldering cleaning operation to prevent early failure of the soldered assembly.

3.3.2.3 No Clean Fluxes (Low Residue/No Residue) This family of fluxes includes both rosin or modified resin fluxes and nonrosin fluxes. The activators used are generally weak organic dicarboxcylic acids.

The low solids rosin/resin based fluxes leave small amounts of residue after soldering which may interfere with bed of nails testing or other post-soldering operations or operating characteristics. They generally have no deleterious impact on reliability and do not need to be removed from the assembly with a post solder defluxing operation.

Other no clean fluxes, leaving no residue, are formulated with no rosin and utilize a mixture of one or more weak dicarboxcylic acids and wetting agents to provide the activation needed to enhance soldering. These fluxes leave little or no residue and do not need to be removed from the assembly with a post solder defluxing operation.

An inert gas atmosphere, such as nitrogen, is often used to enhance the soldering process when using these more benign fluxes.

3.3.3 Cleaning Agent In addition to removing grease, oil, wax, dirt, flux and other debris, cleaning agents should also remove flux residue, ionic, ionizable nonpolar and particulate contaminants. The cleaning agent should not degrade the materials and parts being cleaned. Trichloroethylene and some other chlorinated solvents should not be used on glass-silicone resin laminated material Delamination and surface/component damage may result with their use.

3.3.4 Adhesive Used for securing components in place during soldering should not degrade the solderability of nearby interconnection sites or lead to corrosion or unacceptable insulation resistance properties of the assembly. Insulation testing of adhesives is described in IPC-CA-821.

3.3.4.1 Anisotropic Conductive Adhesive Conducts electricity in one direction only, the Z-axis (between parallel traces). A film of anisotropic adhesive can be placed between the circuit and the components. Heat and pressure are simultaneously applied so that component terminations press down into conductive particles and, in turn, press the particles against the lands. The adhesive holds the component in place upon cooling. Heat may be applied to certain component leads (such as larger gull-wing types). Conversely, convection or direct transfer may heat the circuit. Liquid thermoset adhesive materials are processed differently. The material is coated or printed onto the circuit. The entire board can be covered. Components are conventionally placed and heating them cures the adhesive. Electrical contact is made between the circuit and the components. The conductive particles in the unpopulated areas remain dispersed within the resin so that it serves as an insulating coating.

Caution: Use only with manufacturer’s approved component and land surface finishes. Other finishes may lead to reliable connections (see IPC-3406 and IPC-3408).

3.3.5 Components Should be compatible with all solders, process chemicals, and temperatures used to manufacture the assembly. Components that do not meet these requirements must be given special handling.

3.3.6 Printed Boards Should be in accordance with the requirements of the applicable design and performance specification (see 1.2.3 and Table 1-1).

3.3.7 Board & Lead Finishes Should be uniform and of specified thickness. They should be thoroughly cleaned of all residues, capable of adequate storage life times, and impart solderability to the lead or termination that they cover.

Gold or palladium finishes that could cause embrittlement of the solder connection must be carefully evaluated. Finishes such as immersion gold are viable if the thickness is controlled.

3.3.8 Solderability To achieve acceptable solder connections the surfaces to be joined must be solderable. This is known as solderability.

Good solderability can improve production rates, increase reliability, lower costs and improve joint appearance. Production rates increase significantly if board solder joints do not have to be reworked or touched up. Manual touch ups can damage printed boards and impact long-term reliability.

The solderability of both component leads and printed boards is important. Degradation of either part impedes the formation of good solder joints. The emphasis of the control of solderability has been placed on component leads rather than on printed boards due to the following component characteristics:

• Longer storage times

• More rigorous processing during manufacturing

• Lower cost compared to cost of reworking the PWB

3.3.8.1 Solderability Testing Considerable work on solderability control has been applied to printed boards. This includes both testing for solderability and improving the surfaces to be soldered. Testing solderability is required to successfully handle solderability problems. In the last ten years, many tests have been devised for component leads, terminals and printed boards.

J-STD-002 and J-STD-003 list the current requirements and test methods to be used in accordance with the customers' needs for component leads and wires and printed boards:

3.3.9 Coating

3.3.9.1 Conformal Coating Considerations A thin layer of insulating material that is applied to a printed board assembly. This material closely follows the contours of the board and components. It ''conforms'' to the shape of the assembly, and produces a film of consistent thickness over the entire assembled printed board. Assembled printed boards are frequently given a conformal coating to assist them in functioning under certain environmental conditions. Correctly chosen, and carefully applied, conformal coating helps to protect the assembly from the following hazards:

• Humidity

• Dust and dirt

• Airborne contaminants - e.g., smoke, chemical vapors

• Conducting particles - e.g., metal chip, filing

• Accidental short circuit by dropped tools, fasteners, etc.

• Abrasion damage

• Vibration and shock (to a certain extent)

Conformal coating is not a substitute for good design, or the selection of adequate components and materials. It does, however, assist the designer in producing equipment that performs under hostile conditions. The conformal coating should be compatible with any solder resist used on the assembly. Conformal coatings protect the electrical characteristics of the assembly by doing the following:

• Preventing contamination of the dielectric surface by field soil, which in humid environments can cause electrical leakage.

• Inhibiting the growth of fungus, thereby protecting the electrical characteristics. Even nonnutrient surfaces can support fungus growth when contaminated with field soils such as oil vapor.

• Suppressing electrical flashover between conductors at high altitudes.

The secondary function of conformal coating is to help support the components, relieving the solder joints from carrying the entire mass of the component. Properties to be considered in quality test and/or evaluations:

• Appearance

• Thickness

• Fungus resistance

• Adhesion

• Shelf life

• Pot life

• Abrasion resistance

• Solvent resistance

• Flammability

• Dielectric withstanding voltage

• Moisture resistance

• Thermal shock resistance

• Thermal humidity aging

• Fluorescence

• Resonance

For additional information on conformal coating see IPC-CC-830 and IPC-HDBK-830.

3.4 Handling and Storage This section discusses handling and storage issues such as electrical overstress (EOS), electrostatic discharge (ESD) and storage methods designed to reduce moisture impact on solderability, component cracking/delamination (popcorning) and board damage.

Care must be taken during acceptability inspections to ensure product integrity at all times.

Moisture sensitive component (as defined by IPC/JEDEC J-STD-020 or equivalent documented procedure) must be handled in a manner consistent with J-STD-033 or an equivalent documented procedure.

The following general rules should be practiced when handling printed board assemblies:

- Keep workstations clean and neat.
- Do not eat or drink in the work area. This prevents contamination of the board assemblies.
- Avoid handling the board edge contacts.
- Do not use hand creams and lotions containing silicone since they can cause solderability problems. Lotions formulated specially for use in solder assembly areas are available.
- Do not stack board assemblies. This prevents physical damage to components. The special racks normally provided in assembly areas can create contamination; therefore, changes should be made as frequently as necessary.
- Perform all handling and assembly at an antistatic workstation. Electrostatic discharge may damage sensitive components.

Caution: Cleaning agents may damage certain substrates and unsealed components such as switches, power modules, adjustable devices, etc. Care must be taken to identify and protect these types of components through the cleaning process.

3.4.1 EOS/ESD Electrostatic Discharge (ESD) is the rapid discharge of electrical energy created from electrostatic sources. Electrical energy can cause damage if it comes in proximity of or in contact with sensitive components. Electrostatic Discharge Sensitive (ESDS) components are affected by these high-energy surges. The relative sensitivity of a component to ESD is dependent upon its construction and materials. As components become smaller and operate faster, their sensitivity increases.

Electrical Overstress (EOS) is the internal result of an unwanted application of electrical energy that results in damaged components. This damage can come from many different sources, such as electrically powered process equipment or the handling or processing of components. ESDS components can fail to operate or change in value as a result of improper handling or processing. These failures can be immediate or latent. Additional testing, reworking, or even scrapping can result from immediate failures. The consequences of latent failure are the most serious. Even though the product may have passed inspection and functional testing, it may fail after the customer receives it. Build protection for ESDS components into circuit designs and packaging is important. In the manufacturing and assembly areas, work is often done with unprotected electronic assemblies (such as test fixtures) that are attached to the ESDS components. Removing ESDS items from their protective enclosures only at EOS/ESD safe workstations within Electrostatic Protected Areas (EPA) is another important consideration. This section discusses the safe handling procedures of these unprotected electronic assemblies.

Information in this section is intended to be general in nature. Additional information can be found in ANSI/ESD-S-20.20 and other related documents. This section covers the following subjects:

3.4.1.1 Electrical Overstress (EOS) Damage Prevention Unwanted electrical energy from many different sources could damage electrical components. ESD potentials can cause this unwanted electrical energy. Another source are electrical spikes caused by the tools such as soldering irons, soldering extractors, testing instruments or other electrically operated process equipment. Some devices are more sensitive than others, depending on the design of the device. In general, devices that are smaller or have higher speeds are more susceptible than their slower, larger predecessors are. The purpose or family of the device also plays an important part in component sensitivity. This is because the design of the component can allow it to react to smaller electrical sources or wider frequency ranges. EOS is a more serious problem than it was even a few years ago. It is even more critical in the future.

The susceptibility of the most sensitive component in the assembly must be considered. Applied unwanted electrical energy can be processed or conducted just as an applied signal would be during circuit performance.

Before handling or processing sensitive components, tools and equipment need to be carefully tested to ensure that they do not generate damaging energy, including spike voltages. Current research indicates that voltages and spikes less than 0.5 volt are acceptable. However, an increasing number of extremely sensitive components require that soldering irons, solder extractors, test instruments and other equipment must never generate spikes greater than 0.3 volt.

As required by most ESD specifications, periodic testing may be warranted to preclude damage as equipment performance may degrade with use over time. Maintenance programs for process equipment are also necessary to ensure they do not cause EOS damage.

EOS damage is similar in nature to ESD damage, since both result from undesirable electrical energy.

3.4.1.2 Electrostatic Discharge (ESD) Damage Prevention The best ESD damage prevention is a combination of preventing static charges and eliminating static charges if they do occur. All ESD protection techniques and products address one or both of these issues.

ESD damage is the result of electrical energy generated from either applied or approximate static sources to ESDS devices. The degree of static generated is relative to the characteristics of the source. To generate energy, relative motion is required. This could come from contacting, separation, or rubbing the material. Most of the serious offenders are insulators since they concentrate energy where it was generated or applied rather than allowing it to spread across the surface of the material. Common materials such as plastic bags or Styrofoam containers are serious static generators and as such are not to be allowed in processing areas; especially in static safe/Electrostatic Protected Areas (EPA). Peeling adhesive tape from a roll can generate 20,000 volts. Even compressed air nozzles that move air over insulating surfaces generate charges (see Table 3-1).

Table 3-1 Typical Static Charge Sources

Environment	Source
Work surfaces	Waxed, painted or varnished surfaces Untreated vinyl and plastics Glass
Floors	Sealed concrete Waxed or finished wood Floor tile and carpeting
Clothes and personnel	Non-ESD smocks Synthetic materials Non-ESD Shoes Hair
Chairs	Finished wood Vinyl Fiberglass Nonconductive wheels
Packaging and handling materials	Plastic bags, wraps, envelopes Bubble wrap, foam Styrofoam Non-ESD totes, trays, boxes, parts bins
Assembly tools and materials	Pressure sprays Compressed air Synthetic brushes Heat guns, blowers Copiers, printers

Destructive static charges are often induced on nearby conductors, such as human skin, and discharged into conductors on the assembly. This can happen when a person, having an electrostatic charge potential, touches a printed board assembly. The electronic assembly can be damaged as the discharge passes through the conductive pattern to an ESDS component. Electrostatic discharges may be too low (less than 3500 volts) to be felt by humans, and still damage ESDS components.

Typical static voltage generation is included in Table 3-2.

Table 3-2 Typical Static Voltage Generation

Source	10-20% Humidity (Volts)	65-90% Humidity (Volts)
Walking on carpet	35,000	1,500
Walking on vinyl	12,000	250
Worker at a bench	6,000	100
Vinyl envelopes (Work Instructions)	7,000	600
Plastic bag picked up from the bench	20,000	1,200
Work chair with foam pad	18,000	1,500

3.4.1.3 ESD Damage Prevention - Warning Labels Warning labels are available for posting in facilities and placement on devices, assemblies, equipment and packages to alert people to the possibility of inflicting electrostatic or electrical overstress damage to the devices they are handling. Examples of frequently encountered labels are shown in Figure 3-8.

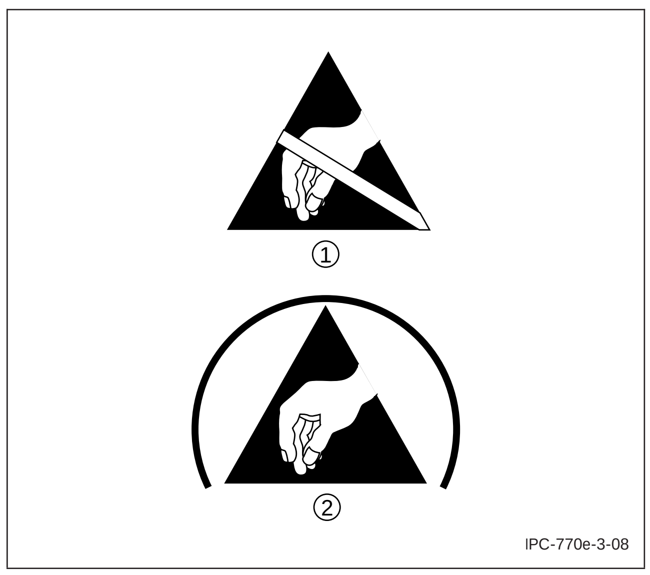


Figure 3-8 Frequently Encountered EOS/ESD Warning Labels

Symbol (1): ESD susceptibility symbol. A triangle with a reaching hand and a slash across it. This symbol indicates that an electrical or electronic device or assembly is susceptible to damage from an ESD event.

Symbol (2): ESD protective symbol. This differs from the ESD susceptibility symbol in that it has an arc around the outside of the triangle and no slash across the hand. This symbol identifies items that are specifically designed to provide ESD protection for ESD sensitive assemblies and devices. Symbols (1) and (2) identify devices or an assembly as containing devices that are ESD sensitive, and must be handled accordingly. These symbols are promoted by

the ESD association and are described in EOS/ESD standard S8.1 as well as the Electronic Industries Association (EIA) in EIA-471 and IEC/TS 61340-5-1.

Note: The absence of a symbol does not necessarily mean that the assembly is not ESD sensitive. When doubt exists about the sensitivity of an assembly, it must be handled as a sensitive device until it is determined otherwise.

3.4.1.4 ESD Damage Prevention - Protective Materials ESDS components and assemblies must be protected from static sources when not being worked on in static safe environments or workstations. This protection could be conductive static-shielding boxes, bags or wraps.

ESDS items must be removed from their protective enclosures only at static safe workstations.

It is important to understand the difference between the three types of protective enclosure materials: (1) static shielding (or barrier packaging), (2) antistatic packaging material and (3) static dissipative materials.

- ***Static Shielding Packaging –*** Prevents an electrostatic discharge from passing through the package and into the assembly causing damage.
- ***Antistatic (Low Charging) Packaging Materials –*** Provides inexpensive cushioning and intermediate packaging for ESDS items. Antistatic materials do not generate charges when motion is applied. However, if an electrostatic discharge occurs, it could pass through the packaging and into the part or assembly, causing EOS/ESD damage to ESDS components.
- ***Static Dissipative Materials –*** Have enough conductivity to allow applied charges to dissipate over the surface relieving hot spots of energy. Parts leaving an EOS/ESD protected work area must be overpacked in static shielding materials, which normally also have static dissipative and antistatic materials inside.

Note: Do not be misled by the color of packaging materials. It is widely assumed that black packaging is static shielding conductive and that pink packaging is antistatic in nature.

While that may be generally true, it can be misleading. In addition, there are many new clear materials now on the market that may be antistatic and even static shielding. At one time it could be assumed that clear packing materials introduced into the manufacturing operation would represent an ESD hazard. This is not necessarily the case now.

Caution: Some static shielding, antistatic materials and topical antistatic solutions may affect the solderability of assemblies, components, and materials in process. Select only noncontaminating packaging and handling materials in-process assemblies and use them with regard for the vendor's instructions. Solvent cleaning of static dissipative or antistatic surfaces can degrade their ESD performance. Follow the manufacturer's recommendations for cleaning.

3.4.1.5 EOS/ESD Safe Workstation/EPA An EOS/ESD safe workstation prevents damage to sensitive components from spikes and static discharges while operations are being performed. Safe workstations should include EOS damage prevention by avoiding spike generating repair, manufacturing or testing equipment. Soldering irons solder extractors and testing instruments can generate energy of sufficient levels to destroy extremely sensitive components and seriously degrade others.

For ESD protection, a path to ground must be provided to neutralize static charges that might otherwise discharge to a device or assembly. ESD safe workstations/EPAs also have static dissipative or antistatic work surfaces that are connected to a common ground. Provisions are also made for grounding the worker's skin, preferably via a wrist strap designed to eliminate charges generated on the skin or clothing. Provisions must be made in the grounding system to protect the worker from live circuitry as a result of carelessness or equipment failure. This is commonly accomplished through resistance in line with the ground path, which also slows the charge decay time to prevent sparks or surges of energy from ESD sources. Additionally, a survey must be performed of the available voltage sources that could be encountered at the workstation to provide adequate protection from personnel electrical hazards.

For maximum allowable resistance and discharge times for static safe operations see Table 3-3.

Table 3-3 Maximum Allowable Resistance and Discharge Times for Static Safe Operations

Reading from Operator Through:	Maximum Tolerable Resistance	Maximum Acceptable Discharge Time
Floor mat to ground	1000 megohms	Less than 1 sec.
Table mat to ground	1000 megohms	Less than 1 sec.
Wrist strap to ground	100 megohms	Less than 0.1 sec.

Note: The selection of resistance values is to be based on the available voltages at the station to ensure personnel safety as well as to provide adequate decay or discharge time for ESD potentials. Examples of acceptable workstations are shown in Figures 3-9 and 3-10. When necessary, air ionizers may be required for more sensitive applications. The selection, location, and use procedures for ionizers must be followed to ensure their effectiveness.

Keep workstation(s) free of static generating materials such as Styrofoam, plastic solder removers, sheet protectors, plastic or paper notebook folders, and employees' personal items.

Periodically check workstations/EPAs to make sure they work. EOS/ESD assembly and personnel hazards can be caused by improper grounding methods or by an oxide

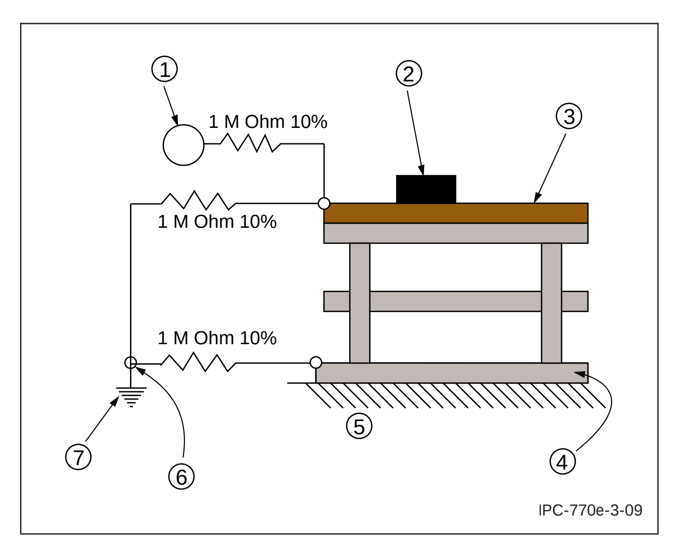


Figure 3-9 Series Connected Wrist Strap

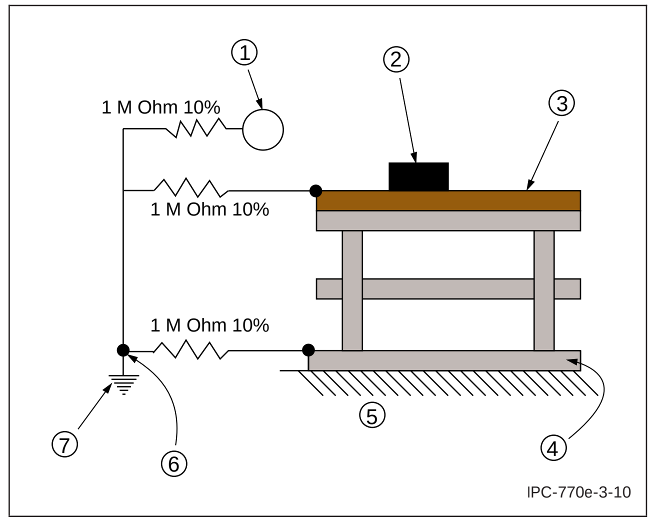


Figure 3-10 Parallel Connected Wrist Strap

build-up on grounding connectors. Tools and equipment must be periodically checked and maintained to ensure proper operation.

Note: Because of the unique conditions of each facility, particular care must be given to ‘‘third wire’’ ground terminations.

Frequently, instead of being at workbench or earth potential, the third wire ground may have a ‘‘floating’’ potential of 80 to 100 volts. This 80 to 100 volt potential between an electronic assembly on a properly grounded EOS/ESD workstation/EPA and a third wire grounded electrical tool may damage EOS sensitive components or could cause injury to personnel. Most ESD specifications also require these potentials to be electrically common. The use of ground fault interrupter (GFI) electrical outlets at EOS/ESD workstations/EPAs is highly recommended.

3.4.2 Moisture Sensitivity Plastic bodied components are susceptible to absorption and retention of moisture. Component manufacturers should assign components to a moisture sensitivity level using IPC/JEDEC J-STD-020A. This level of sensitivity determines the method of preservation required assuring that the components do not crack or delaminate (popcorn) during the manufacturing process. IPC/JEDEC J-STD-035 provides a test method for determining if damage has occurred during the manufacturing process. IPC-9501, 9502, 9503, and 9504 provide guidance on conditioning of components prior to assembly. IPC/JEDEC J-STD-033 provides detail instruction on handling moisture sensitive devices.

Printed circuit boards are also susceptible to moisture absorption and can exhibit damage as a result of that moisture during the assembly process. Because of the complexity and variables associated with boards, the user needs to determine the specific storage or baking time and temperature requirements.

3.4.3 Storage The preservation of solderability and the protection of parts and assemblies from handling and ESD damage should be a vital control aspect of the manufacturing process of printed board assemblies. Printed boards should be protected before shipping or transportation to the destination where they are received and assembled.

3.4.3.1 Storage Material Care should be exercised to assure that packaging materials do not contain additives or surface treatments that deteriorate solderability or degrade the insulation properties of components, boards or assemblies.

3.4.3.2 Bags One of the most common forms of protection for bare boards is an antistatic bag wrapped with a moisture barrier and then cushioning material.

Ensure the boards are thoroughly cleaned before being packaged and that the atmosphere in which the boards are packed is reasonably dry. Sealing moisture or a contaminated environment within a bag can affect the solderability and moisture content of the boards.

Printed boards, components and hardware are frequently placed in their original containers and put on a shelf until they are required. Some consideration should be given at this point to the packing material in use. If the manufacturer did not provide a protective material, it is advisable to repackage.

Parts should not be stored in open containers exposed to environment that may cause the parts to oxidize (for example, dust and air pollutants).

Inventory control should carefully handle the parts with a ‘‘first in-first out’’ policy.

Components and boards should not be left exposed overnight or over weekends. This causes dust and debris from the atmosphere to accumulate.

3.5 Material Movement Systems

3.5.1 Transporters One method of providing material to the production stations is accomplished by means of the transporter system controlled by a central dispatch area. Typically the transporter consists of two levels. The upper level dispatches the work while the lower level returns completed work. Strategically placed photocells on the return conveyer read bar code labels on the tote box to provide automatic work-in-progress (WIP) status to a central computer. Static-free conveyer belts and the grounding of machinery should provide protection for ESD sensitive components.

Personnel must use ESD protection at all times when touching devices or assemblies.

3.5.2 Racks and Carriers Store assembled boards between component mounting and soldering. When storing the assembled boards, covering the racks with an approved material to keep them out of the way of dust and debris is recommended.

Frequently, problems due to improper storage lead to future failures. These may show up in the final assembly testing operation or in the form of field failures.

4 COMPONENT GUIDELINES

This section contains a general introduction to the kinds of components that are discussed in detail in the following chapters. Common characteristics of components, component selection and general issues are considered here.

Components are selected for electrical, thermal, or mechanical characteristics determined by the requirements of the contents of the package. The material composition, finish and configuration of both the body and the terminations of a component must be considered in the choice of assembly methods.

All components must be qualified for the assembly processes to be used. The physical dimensions of the component must adequately mate with the physical handling devices of the placement equipment. Soldering or other high temperature processes used must not degrade the parts, physically or electrically. Also, the parts must be able to tolerate exposure to the chemicals used in adhesive bonding, soldering, cleaning or any other chemical processing.

Electronic components come in a great variety of package styles and shape. This relates not only to the electrical functions that the components perform but sometimes the same function is available in different packaging configurations.

Component selection should consider the following factors when applicable:

- Electrical Characteristics
- Electrical Performance
- Mating Forces
- Environmental Requirements
- Durability
- Repairability
- Manufacturing Methods
- Mechanical Requirements
- Thermal Requirements
- Electrical Environment
- Placement/Attachment Equipment
- Polarization
- Cleaning
- Corrosion
- Part Identification/Verification
- Special considerations (heat sensitive, unsealed, etc.)

4.1 Component Characterization and Classes There are two classes of components:

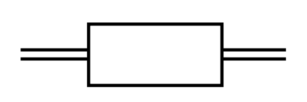
- Through Hole (see Figure 4-1)
- Surface Mounted (see Figure 4-2)

Note: Components listed in Figures 4-1 and 4-2 are not all-inclusive, and not intended to represent all types of components.

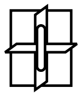
4.1.1 Axial-Leaded Components Discrete axial-leaded devices are two-leaded board mounted components that have the leads exiting from the ends of the component along the axis of the components. They are considered suitable for automatic component insertion. The most common axial-leaded devices are resistors, capacitors and diodes. Detailed description of axial leaded components is contained in Section 2.

4.1.2 Radial-Leaded Components Two or more-leads that exit from one side of the component. Sometimes this side is on the perimeter of the package and sometimes it is the bottom of the component. The body shapes vary from simple disc-shaped capacitors to transistor outline (TO) shapes (can) to parallel-leaded devices such as dual or single in-line packages. Generally, active semiconductor devices or arrays of two terminal devices can be packaged in multileaded radial configurations. The details of multileaded radial components are contained in Section 2.

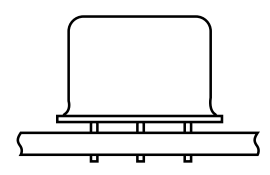
4.1.3 Chip Components Comprise a wide variety of two-terminal devices for surface mount attachment. Some of the chip components have formed metal leads for attachment but most are simple ceramic devices with plated or solder dipped terminations that are integral to the body of the component. Chip components are small. They are



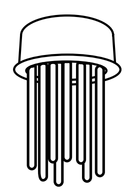
1. Axial Parts (2 Leads)



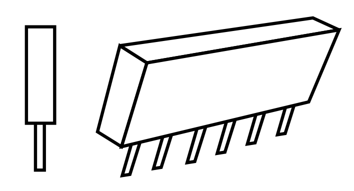
2. Radial Parts (2 Leads)



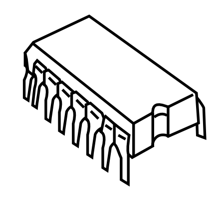
3. Radial Parts (3 or more Leads)



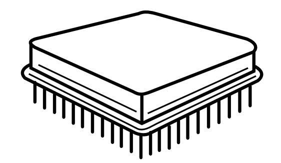
4. TO IC



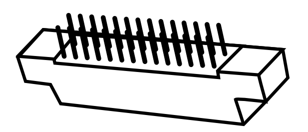
5. Single In-line Packages (SIP)



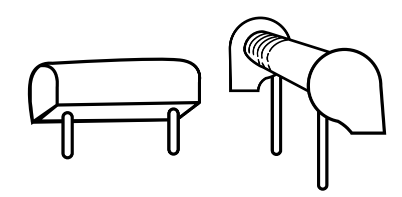
6. Dual In-line Packages



7. Pin Grid Arrays



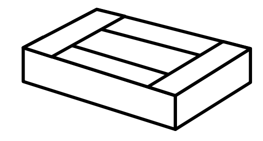
8. Sockets and Connectors



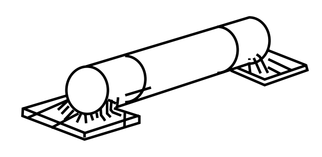
9. Others (Transformers, Chokes, Coils, Trim Pots, etc.)

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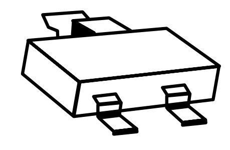
Figure 4-1 Through-the-Board Component Types



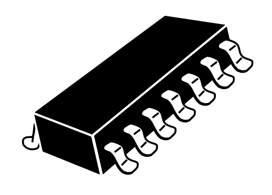
10. Chip Component, Rectangular or Square



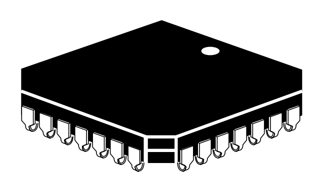
11. Cylindrical End Cap - Metal Electrode Leadless Face (MELF)



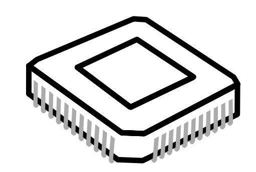
12. Small - Outline Transistors (SOT)



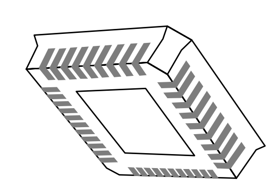
13. Small - Outline IC (SOIC)



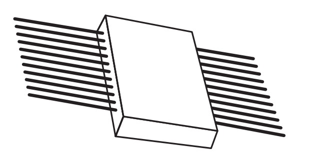
14. Plastic Leaded Chip Carrier (PLCC)



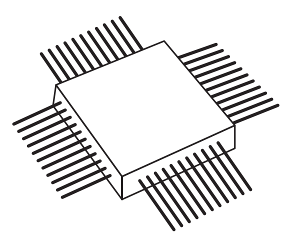
15. Ceramic Leaded Chip Carrier (CLCC)



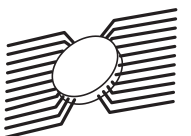
16. Ceramic Leadless Chip Carrier (LCCC)



17. Flat Pack



18. Quad Pack



19. Other

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Figure 4-2 Some Surface Mount Component Types

designed and packaged for automatic component handling. The details of chip components are contained in Section 12 *Component Characteristics Surface Mount.*

4.1.4 Small Outline Components (SOs) A family of two or more lead plastic post-molded components intended for surface mount attachment. Details of SO components are contained in Section 12.2.1.5.

4.1.5 Multiple-Ribbon-Lead Components Ribbon-leaded components (flat-pack, gull-lead, and J-lead) have flat wire ribbon leads that are arrayed around the perimeter of the component. They are frequently used to package integrated circuits. Ribbon-leaded component details are contained in Sections 12 and 14.

4.1.6 Chip Carriers Currently the most common multi-leaded surface mount package. The terminations are arrayed around the perimeter of the rectangular body. They can come as either formed metal leads or pads that are integral to the body of the component. For printed board mounting, most chip carrier leads are located on 1.27 mm centers, but newer designs are considering 0.635 mm and smaller spacing between leads. The small lead spacing and the large number of leads can require special assembly procedures. Chip carrier package details are contained in Section 14.

4.1.7 Unpackaged Semiconductors This type of component includes all semiconductor devices that are not in individual discrete packages. They may consist of individual semiconductor dice that have termination bonding pads or they may be semiconductor dice bonded to flexible substrates, such as TAB, to aid in their handling and interconnection. These components are used primarily with chip-on-board technology as described in Section 18.

4.1.8 Tape Automated Bonding (TAB) Involves the automated bonding of semiconductor devices (dies) to a flexible lead frame in tape and reel format. The devices are delivered to the assembly operation on tape where the individual devices and part of the interconnecting lead frame are excised, the leads formed and the devices directly mounted to a printed board structure. TAB devices are frequently encapsulated after mounting to the printed board structure.

4.1.8.1 PGA Pad Grid Arrays Also known as Land Grid Arrays, these are surface mount packages where the interconnections are distributed in an area array on the bottom of the package. The interconnections are typically solder columns connecting lands on the bottom of the package to a matching set of lands on a printed board structure beneath it. Details of Pad Grid Arrays are contained in Section 15, *Guidelines for High Pin Count Area Array Component Mounting.*

4.1.8.2 Pin Grid Arrays Form a class of very high input/output (I/O) through board mount integrated circuit package. The leads are arranged in a solid area-filling array across the bottom of the package, frequently with space left free under the chip mount area. Details of Pin Grid Array packages are contained in Section 15.

4.1.9 Area Array Components The area array package for semiconductors adapts a metallized circuit pattern applied to a dielectric structure. To this structure, the semiconductor die (a) is attached either to the top or bottom surface. On the underside of the dielectric is an array pattern of metallized lands that will provide a means for both mechanical and electrical interface between the package body and a mating feature such as a printed board. The surface of the dielectric that contains the die may be encapsulated by various techniques to protect the semiconductor. Refer to IPC-7095, Design and Assembly Implementation for Ball Grid Arrays.

4.1.9.1 The Ball Grid Array (BGA) The ball grid array is a surface mount package that utilizes alloy spheres and reflow solder processing to provide a mechanical and electrical interface between the package and the circuit structure. Six contact pitch formats have been established for BGA; 1.50 mm, 1.27 mm, 1.00 mm, 0.80 mm, 0.65 mm and 0.50 mm. Contact spacing of less than 1.00 mm is defined as fine-pitch BGA (FBGA).

4.1.10 Connectors Form the means to interconnect between a printed board structure and another level of interconnection with a separable connection. Connectors between printed boards and cables, backplanes and special printed board structures are common. Frequently connectors consist of a molded plastic housing that contains formed metal contacts. Connectors can be either through board or surface mount assembled. Connector details are contained in Section 14.

4.1.11 Sockets Form of connector used to make separable contact between a printed board structure and the terminations (leads) of a component. Sockets are frequently assembled with the same technologies used for components. Details of sockets are contained in Sections 11 and 14. (Press fit components are not addressed in this series of documents.)

4.1.12 Electromechanical and Interconnect Components Other board mounted components, such as pins, wires, terminals, and mechanical hardware comprise a wide set of parts that are assembled to printed wiring products to enhance the interconnection capabilities and to interface

with housings, supports, test equipment and other peripheral structures. The details of these special components are contained in Section 15.

4.2 Component Packaging/Delivery Systems There are a variety of component packaging methods. These include tape and reel, waffle trays, and tubes, as well as bulk pack. The sectional documents address unique guidelines for specific component types.

4.3 Lead/Termination Finishes Finishes on the leads of leaded component packages and on the metallized terminations of leadless packages, whether for through-hole or surface mounting, preserve and assure the solderability of the interconnection surfaces without decreasing the assembly yield or the attachment reliability. Frequently, solder joints cannot be visually inspected because of their sheer numbers and are physically inaccessible. The large number of solder joints makes it imperative that the solderability of the component I/Os be positively assured prior to assembly. The lead finish that accomplishes this is fused or reflowed tin or solder. The solder coating can be obtained either by solder dipping or tin/lead plating with a subsequent reflow process. It might be necessary to remove excess solder, which could interfere with the assembly or socketing process, with a hot air knife or similar method.

Gold and silver form brittle intermetallics with the tin in solder causing solder joint reliability problems. It is important to know the amount of precious metal plating on the leads as provided by the supplier. It may be necessary to reduce the gold or silver thickness through a tinning operation to assure reliability of the connection.

Caution should be used when leads are coated with tin or tin/lead plating without reflowing prior to assembly because the plating does not always assure solderability. Organic materials that are sometimes co-deposited during the plating process can also cause poor solderability.

In addition, some user specifications require fusing of the tin plate to eliminate the possibility of tin whisker growth.

The foregoing considerations are more critical for surface mounting than for through-hole mounting. Through-hole mounting provides considerable margin because of the mechanical anchoring of the leads and the larger solder volumes.

5 PACKAGING AND INTERCONNECTING (PRINTED BOARD) STRUCTURES

Printed board structures include conventional and modified organic printed boards, inorganic ceramic printed boards, and supporting plane/core structures. Design requirements for printed board structures are described in the IPC-2220 Series, and performance requirements are described in the IPC-6010 Series.

Many different board types can be used to mount intermixed assemblies. The material used to manufacture the printed board plays a large role in the component mounting techniques that may be used to place parts on the printed board structure or board. Printed board design is detailed in the IPC-2220 Series.

5.1 Printed Board Characterization and Classes There are three basic types of printed circuit (printed wiring) boards, all of which can be manufactured with rigid or flexible materials in a variety of methods (see 1.2.3). The three types are listed below in ascending order of interconnection wiring and component density:

- Single-sided with conductors on only one surface of a dielectric (insulating) base.
- Double-sided with conductors on both sides of a dielectric base, usually interconnected by plated-through or otherwise reinforced holes.
- Multilayer-boards with three or more conductor layers separated by dielectric material, usually interconnected by plated-through interlayer holes.

The single-sided board is used for relatively unsophisticated circuitry. They are applicable when circuit types and circuit speeds do not demand unusual electrical characteristics.

Double-sided boards are required for more complex, denser circuit types requiring interconnecting layers.

The requirements for high speed circuits in computer and space industries, with a requirement for a still further increase in package density, has lead to the development of multilayer boards.

All printed boards have an insulating base often referred to as the dielectric or laminate. Laminate bases for single-sided, double-sided or multilayer printed boards can be either ‘‘rigid’’ or ‘‘flexible.’’

5.1.1 Rigid Laminate Boards The boards are selected according to physical, thermal and electrical requirements. Some base materials are ‘‘punchable,’’ enabling low-cost hole formation, thus making them popular for single-sided board use. However, their dimensional stability is unsuitable for making plated-through-hole boards. The more expensive glass-epoxy laminates have good dimensional stability, usually making them the choice for plated-through-hole, double-sided and multilayer boards. Glass-epoxy is not as ‘‘punchable’’ as the other laminate types; therefore, holes are usually drilled. Other laminate types are available for high temperatures, high frequencies and other special requirements.

5.1.2 Flexible Laminate Boards When flexible printed board types are used for surface mounting, through hole mounting or intermixed assemblies, the component-mounting task may become more difficult, depending on

the structure of the detailed assembly. Usually, stiffeners or other rigid sections of the flexible board are provided to insure the proper surface for component mounting. In addition, flexible printed boards usually take many different shapes and special fixturing may be required in order for the component assembly equipment to adequately mount and attach electronic parts.

5.1.3 Metal-Core Boards These types of products, due to their mechanical rigidity, make the component-mounting task somewhat easier. However, the thermal characteristics of the interconnection structure require that the soldering or attachment technique consider the impact that the thermal mass has on the solder joint solidification. Tables 5-1a-d provide a comparison of the advantages and disadvantages of many of the available printed board structures.

5.2 Supporting-Plane Printed Board Structures Supporting metallic or nonmetallic planes can be used with conventional printed boards or with customer processing to enhance printed board properties. Depending on the results desired, the supporting plane could be electrically functional or not. It could also serve as a structure stiffener, heatsink and/or CTE constraint.

5.2.1 Printed Board Bonded to Support Plane (Metal or Nonmetal) This is a conventional thin printed board that has been fabricated and bonded with a rigid adhesive insulation to a supporting plane such as metal (Figure 5-1) or graphite-fiber resin composite. It can create a printed board structure with controlled thermal expansion in the X and Y-axes. Depending on its properties, the supporting plane can improve rigidity, thermal conductivity, etc. However,

Table 5-1a Packaging and Interconnecting Structure Comparison

Organic Based Substrates	Major Advantages	Major Disadvantages	Comments
Epoxy Fiberglass	Substrate size, weight, reworkable, dielectric properties, conventional board processing.	Thermal conductivity, X, Y and Z axis CTE.	Because of its high X-Y plane CTE, limited to environments and applications with small changes in temperature and/or small packages.
Polyimide Fiberglass	Same as Epoxy Fiberglass plus high temperature Z axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, X and Y-axis CTE, moisture absorption.	Same as Epoxy Fiberglass.
Epoxy Aramid Fiber	Same as Epoxy Fiberglass, X-Y axis CTE, substrate size, lightest weight, reworkable, dielectric properties.	Thermal conductivity, X and Y-axis CTE, resin microcracking, water absorption.	Volume fraction of fiber can be controlled to tailor X-Y CTE. Resin selection critical to reducing resin microcracks.
Polyimide Aramid Fiber	Same as Epoxy Aramid Fiber, Z-axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, X and Y-axis CTE, resin microcracking, water absorption.	Same as Epoxy Aramid Fiber.
Polyimide Quartz (Fused Silica)	Same as Polyimide Aramid Fiber, Z-axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, X and Y-axis CTE, Z-axis CTE, drilling availability, cost, low resin content required.	Volume fraction of fiber can be controlled to tailor X-Y CTE. Drill wear out higher than with fiberglass.
Fiberglass/Aramid Composite Fiber	Same as Polyimide Aramid Fiber, no surface microcracks, Z-axis CTE, substrate size, weight, reworkable, dielectric properties.	Thermal conductivity, X and Y-axis CTE, water absorption, process solution entrapment.	Resin microcracks are confined to internal layers and cannot damage external circuitry.
Fiberglass/Teflon Laminates	Dielectric constant, high temperature.	Same as Epoxy Fiberglass, low temperature stability, thermal conductivity. X and Y-axis CTE.	Suitable for high speed logic applications. Same as Epoxy Fiberglass.
Flexible Dielectric	Light weight, minimal concern to CTE, configuration flexibility.	Size.	Rigid-flexible boards offer trade-off compromises.
Thermoplastic	3-D configurations, low high-volume cost.	High injection-molding setup costs.	Relatively new for these applications.

Table 5-1b Packaging and Interconnecting Structure Comparison

Nonorganic Based Substrates	Major Advantages	Major Disadvantages	Comments
Alumina (Ceramic)	CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors.	Substrate size, rework limitations, weight, cost, brittle, dielectric constant.	Most widely used for hybrid circuit technology.

Table 5-1c Packaging and Interconnecting Structure Comparison

Supporting Plane	Major Advantages	Major Disadvantages	Comments
Printed Board Bonded to Plane Support (Metal or Nonmetal)	Substrate size, reworkable, dielectric properties, conventional board processing. X-Y axis CTE, stiffness, shielding, cooling.	Weight.	The thickness/CTE of the metal core can be varied along with the board thickness, to tailor the overall CTE of the composite.
Sequential Processed Board with Supporting Plane Core	Same as board bonded to supporting plane.	Weight.	Same as board bonded to supporting plane.
Discrete Wire	High-speed interconnections, good thermal and electrical features.	Licensed process. Requires special equipment.	Same as board bonded to two-expansion metal support plane.

Table 5-1d Packaging and Interconnecting Structure Comparison

Constraining Core	Major Advantages	Major Disadvantages	Comments
Porcelainized Copper Clad Invar	Same as Alumina.	Reworkability, compatible thick film materials.	Thick film materials are still under development.
Printed Board Bonded With Constraining Metal Core	Same as board bonded to supporting plane.	Weight, internal layer registration.	Same as board bonded to supporting plane.
Printed Board Bonded to Low Expansion Graphite Fiber Core	Same as board bonded to low expansion metal cores, stiffness, thermal conductivity, low weight.	Cost.	The thickness of the graphite and board can be varied to tailor the overall CTE of the composite.
Compliant Layer Structures	Substrate size, dielectric properties, X-Y axis, CTE.	Z-axis CTE, thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

the printed board must be thin enough to preclude warping of the assembly or else the board should be bonded to both sides of the plane (see 5.3.2). The printed board portion of the printed board structure can be either unpopulated or completely assembled and tested prior to being bonded. However, components can only be mounted to one side of the printed board. Also, the support is not normally electrically connected to the printed board.

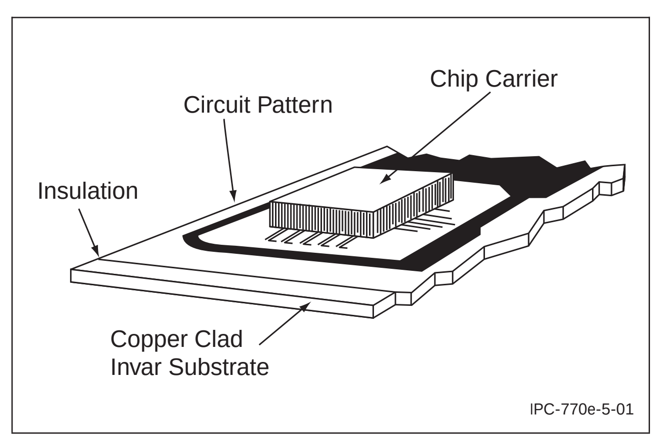


Figure 5-1 Printed Board Bonded to Supporting Plane

5.2.2 Sequentially-Processed Structures with Metal Support Plane High-density, sequentially processed, multilayer printed board structures are available with organic dielectrics of specific thickness, ultrafine conductors, and solid plated vias for layer-to-layer interconnections with thermal lands for heat transfer, all connected to a low-CTE metal support heatsink. Thus, this technology combines laminating materials, chemical processing, photolithography, metallurgy, and unique thermal transfer innovations, such that it is also appropriate for mounting and interconnecting bare integrated circuit chips, as shown in Figure 5-2.

The major advantage of this system is that the vias can be as small as 0.20 mm square and conductor widths can range from 0.12 to 0.20 mm for high interconnection density. Thus, most applications can be satisfied with two signal layers with additional layers for power and ground.

5.2.3 Discrete-Wire Structures with Metal Support Plane Discrete-wire printed board structures have been developed specifically for use with surface mounted components, as shown in Figure 5-3. These structures are usually built with a low-expansion metal support plane that also offers good heat dissipation.

The interconnections are made by discrete 0.06 mm diameter insulated copper wires precisely placed on a 0.03 mm grid by numerically-controlled machines. This geometry results in a low-profile interconnection pattern with excellent high-speed electrical characteristics and a density normally associated with thick-film technology.

The wiring is encapsulated in a compliant resin to absorb local stresses and dampen vibrations. Copper vias 0.25 mm in diameter provide electrical access to the conductors. The small via size can be accommodated in the component-attachment land, thus eliminating the need for fan-out patterns when using components with terminals on centers as close as 0.6 mm, and allowing very-high packaging densities.

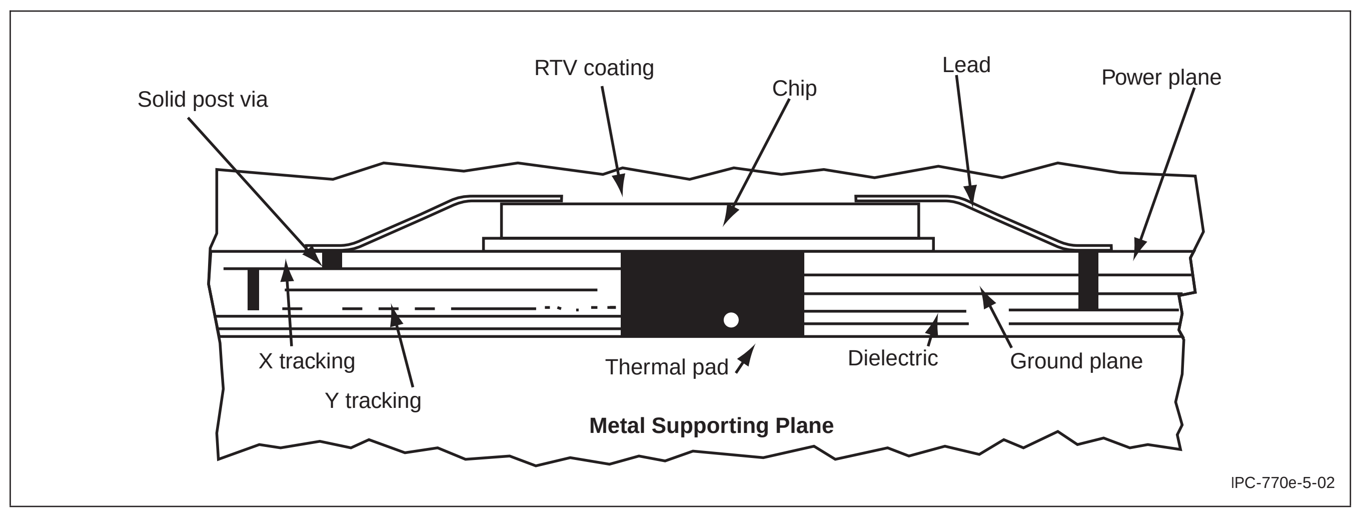


Figure 5-2 Sequentially Processed Structure with Supporting Plane

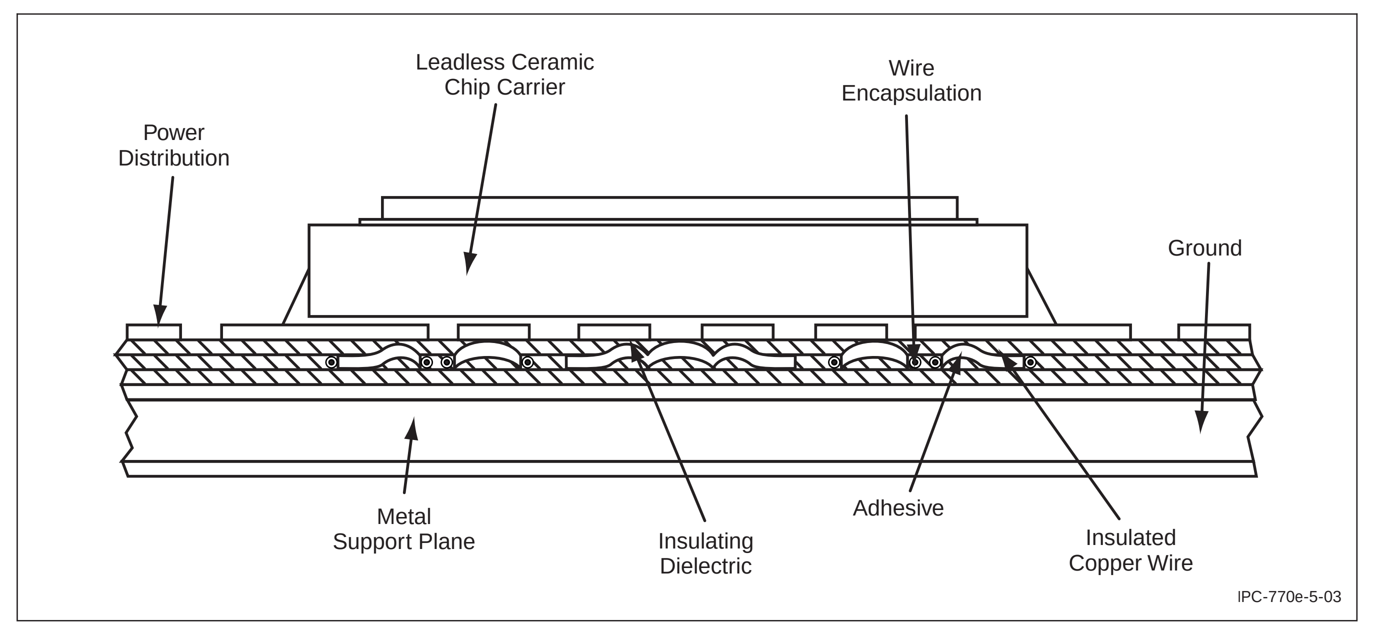


Figure 5-3 Discrete-Wire Structure with Low-Expansion Metal Support Plane

5.2.4 Flexible Printed Board with Metal Support Plane Another arrangement for a printed board structure with leadless components involves conventional fine-line polyimide flexible printed wiring, as shown in Figure 5-4. These assemblies can be constructed in multilayer form while retaining the low-modulus feature that reduces residual strain at the solder joints. Furthermore, lasers can drill very fine holes in the thin printed wiring laminate. These holes can be plated-through or filled with solid copper, as required.

To retain inherent flexibility while dissipating head from the solder joint, cutouts in the flexible circuit accommodate pillars from the metal heatsink support plane. Although this appears to be heavy and cumbersome, if the heatsink baseplates are made from thin sheets of aluminum, the resulting density of the combined circuit/heatsink assembly might actually be less than other constructions.

5.3 Constraining Core Printed Board Structures As with supporting-plane printed board structures, one or more supporting metallic or nonmetallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core printed board structures.

5.3.1 Porcelainized-Metal (Metal Core) Structures An integral core of low-expansion metal (e.g., copper-clad Invar) can reduce the CTE of porcelainized-metal printed board structures so that it closely matches the CTE of the ceramic chip carrier. Also, the printed board structure size is virtually unlimited. However, the low melting point of the porcelain requires low-firing-temperature conductor, dielectric and resistor inks.

A number of composite printed board structures use leadless components. An integral material with a lower CTE than that of the printed boards controls the CTE of these structures.

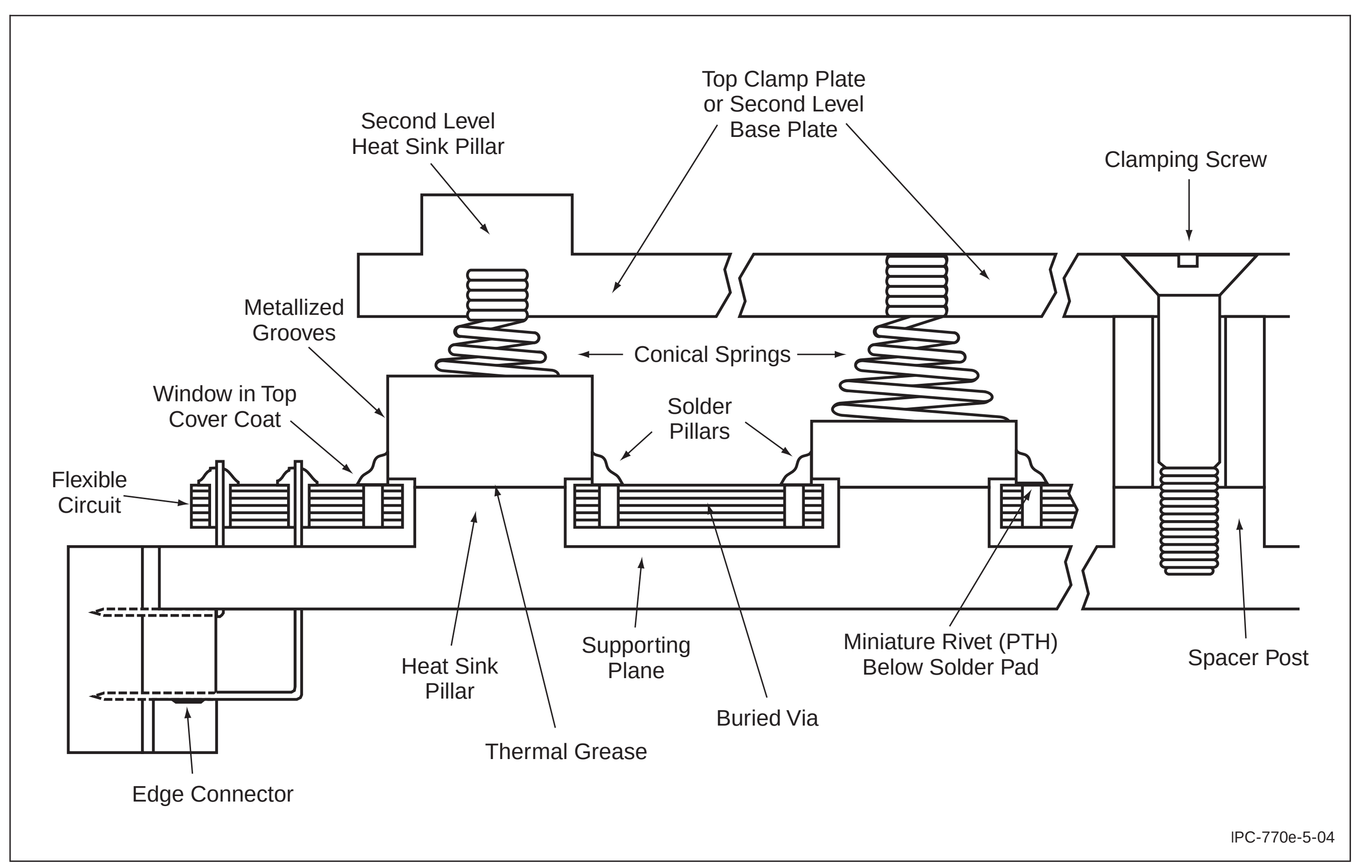


Figure 5-4 Flexible Printed Board with Metal Support Plane

5.3.2 Printed Board with Constraining (Not Electrically Functioning) Core Can be used for high-density, low-warpage printed board structures. The core acts as a heat-sink, but in this case is not electrically functional. For optimum density with this approach, use a multilayer construction with a centrally located predrilled, low-CTE core (see Figure 5-5). The holes in the core are filled with a compatible resin prior to lamination and the printed board structure completed with conventional fabrication techniques.

Molybdenum can be used as the core in these printed board structures for special applications that require inherent stiffness in extreme environments. However, molybdenum and copper-clad Invar are difficult materials to fabricate using conventional processes. Graphite can be used where thermal conductivity per unit of weight is important.

5.3.3 Printed Boards with Electrically-Functional Constraining Cores More conventional multilayer printed boards can be made as printed board structures with thin, 0.1 to 0.25 mm, copper-clad Invar as electrically-functional ground and power planes. After the planes have been predrilled they are located in a symmetrical arrangement within the lay-up and subsequently laminated as an integral part of the multilayer printed board structure (Figure 5-6). Varying the composition and thickness of the planes can tailor the overall CTE of the structure.

5.3.4 Printed Board with Constraining Core A constraining fiber resin composite internal plane in a conventional printed board can modify thermal expansion in the X and Y-axes improve rigidity and improve thermal conductivity, depending on the properties and location of the supporting plane. These constraining fibers can be graphite, Kevlar, quartz, etc. The very high modulus of these materials requires a balanced construction to prevent bowing or twisting (see Figures 5-7 and 5-8 for typical construction). Graphite's high cost is justified if low weight is critical. Graphite is conductive; therefore via holes must be drilled oversize and then resin filled prior to final via hole drilling. Graphite allows excellent CTE tailoring. Kevlar and quartz fibers require modified fabrication techniques due to their mechanical properties.

5.4 Other Mounting Structure Materials and Considerations

5.4.1 Heat Sinks Devices used to absorb and/or transfer heat away from heat sensitive parts. Heat sinks come in many styles, shapes, and sizes and may be designed for mounting on printed boards, on a component or a series of components. They can be mounted by riveting/bolting to the component or the circuit board or by clipping to a mounted component. Some common types are depicted in Figure 5-9.

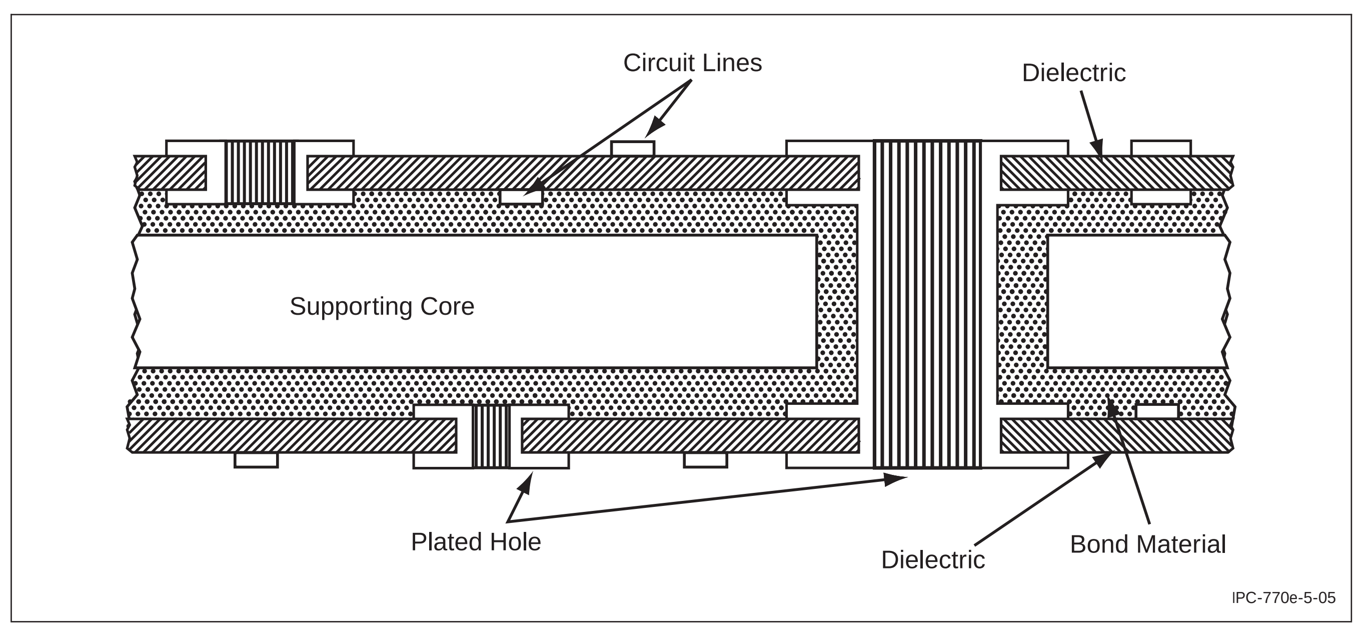


Figure 5-5 Printed Board with Supporting Plane (Not Electrically-Functional Constraining Core)

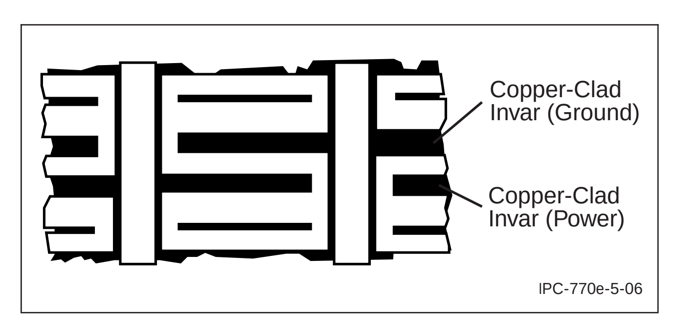


Figure 5-6 Multilayer Printed Board Structure with Copper-Clad Invar Power and Ground Planes (Electrically-Functional Constraining Cores)

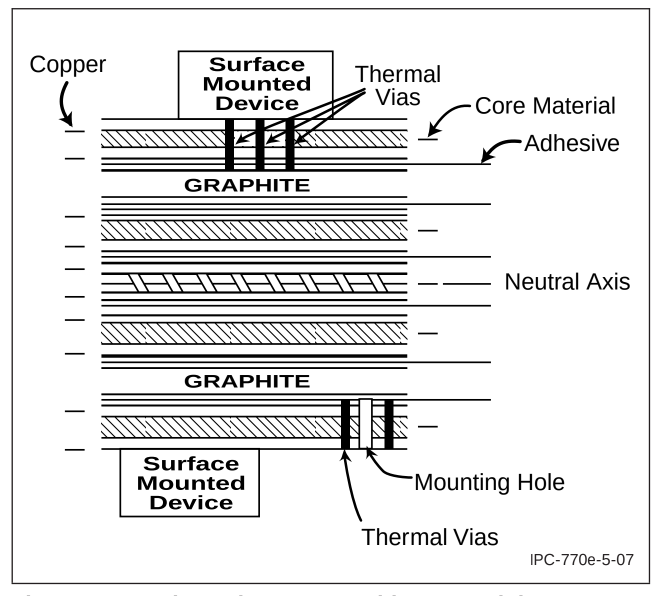


Figure 5-7 Balanced Structure with Constraining Core not at Neutral Axis

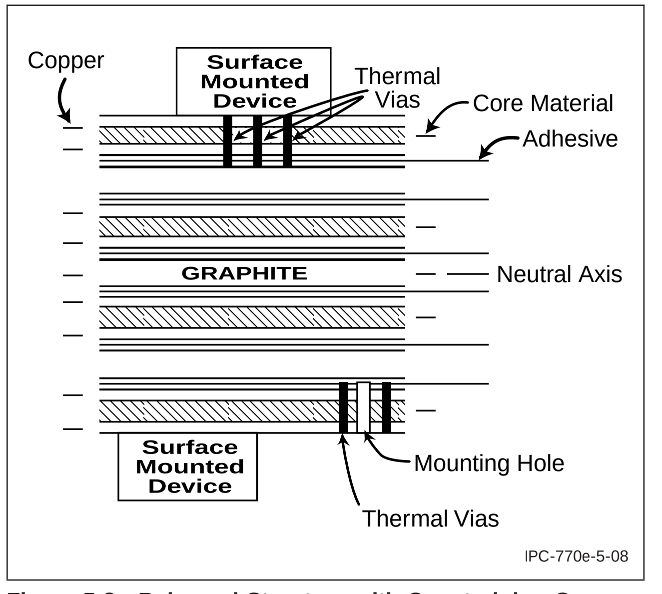


Figure 5-8 Balanced Structure with Constraining Core on Neutral Axis not at Neutral Axis

To facilitate heat sinking of components that must be electrically insulated from heat sinks, chassis, washers, etc., thermally conductive epoxy compounds and adhesives, silicone grease, silicone rubber and other materials are available. The silicone rubber and other sheet material are usually provided in the shape of the various devices. Forced air convection can improve the effectiveness of heat sinks. Heat pipes are also used for heat sinking, spreading hot spots or causing several components to operate at the same temperature. Recently, heat sinks have become available which permit mounting of the active component/heat sink combination. These can then be mounted to the printed board. Some of these heat sinks contain provisions that

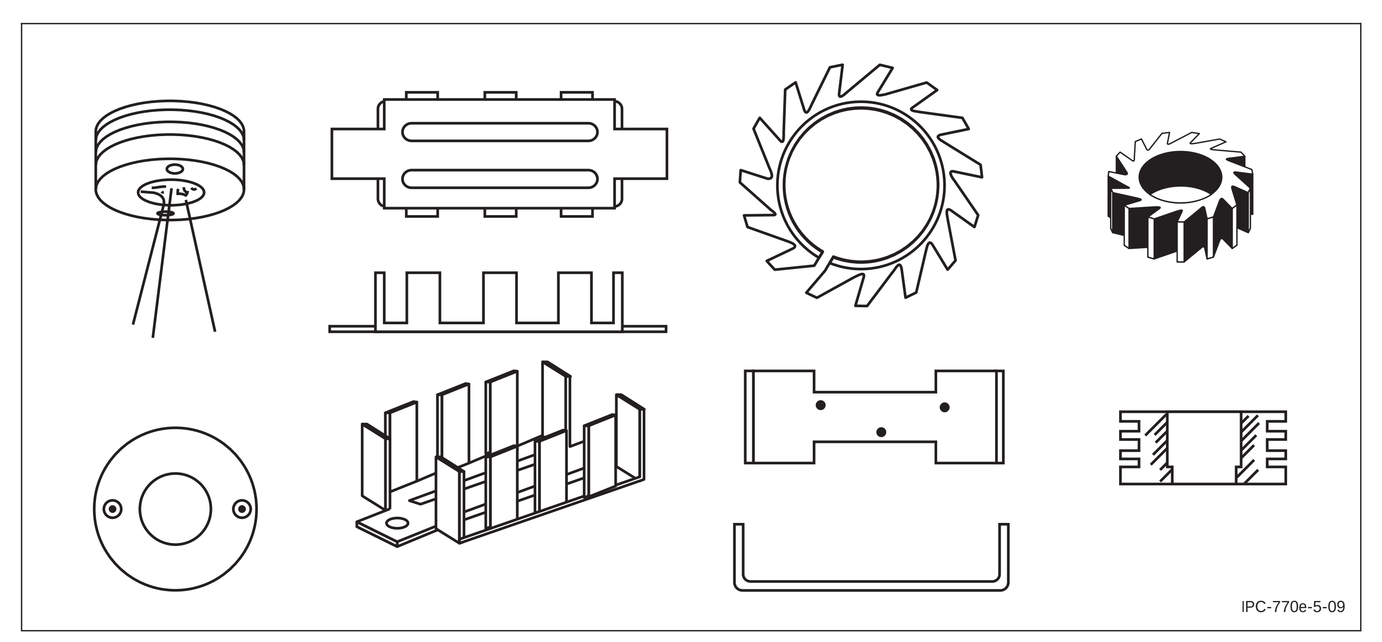


Figure 5-9 Common Component Heat Sinks

permit the heat sink and component leads to be soldered directly to the board.

5.4.2 Spacers Maintain a component above the mounting surface for electrical clearance, increase soldering and cleaning capabilities, improve air flow on heat dissipative parts, provide mechanical support, and facilitate and minimize thermally cleaning-induced stresses.

Spacers are manufactured from nonconductive materials (plastic, nylon, and Teflon), materials that do not dissolve during the cleaning process. Spacers are usually used on multileaded radial devices (three or more leads), such as transistors, or amps, potentiometers, etc. See Figure 5-10 for examples.

5.4.3 Component-Lead Spreaders The use of multiple lead can spreaders, Figure 5-11, serves a similar function for offset can mounting as do spacers for straight-through can mounting. Leads may be terminated in the clinched or unclenched lead method.

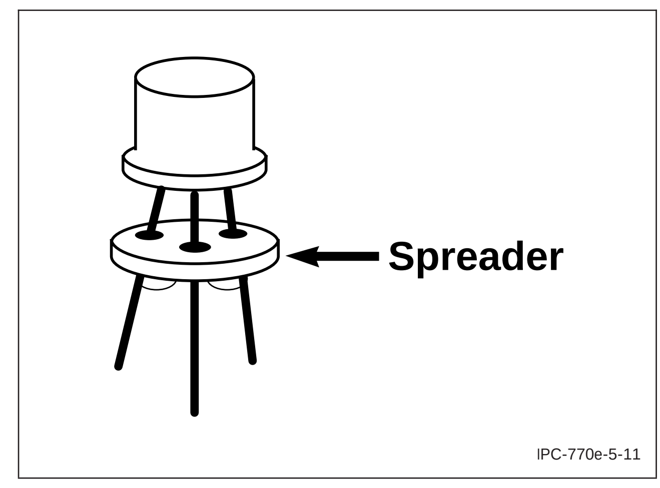


Figure 5-11 Can Mounting Spreader

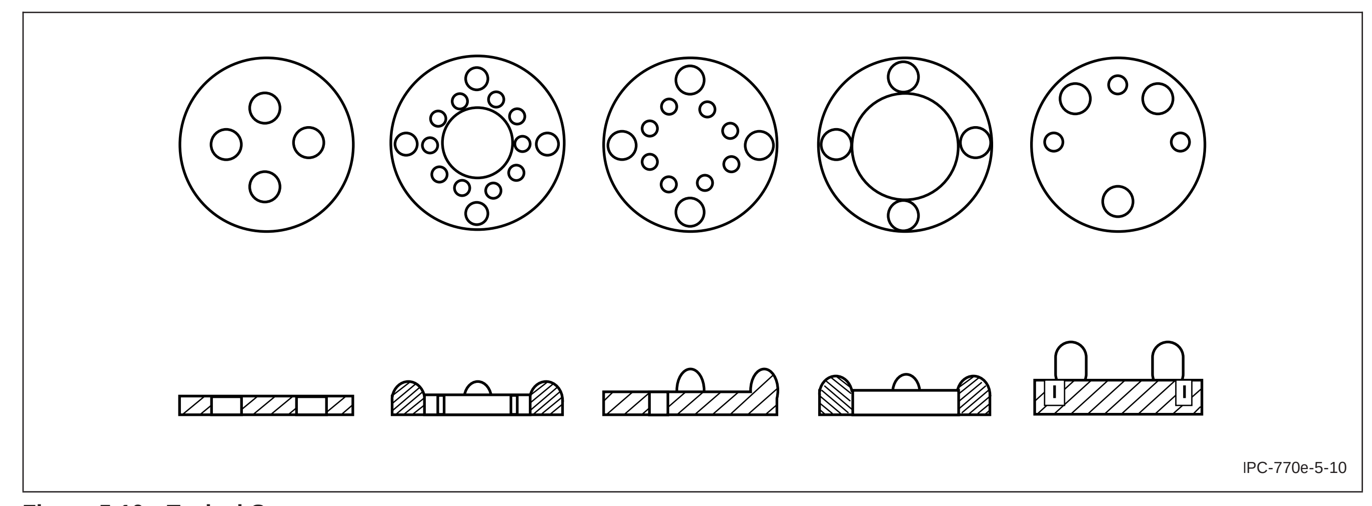


Figure 5-10 Typical Spacers

5.4.4 Thermally Conductive Insulators The most common method of obtaining thermally conductive insulators has been by the use of a silicone grease and mica or plastic film on printed board assemblies which must be cleaned and conformally coated. The use of silicone grease can cause cleaning and coating adhesive problems. Thermally conductive insulators made of silicone rubber and fiberglass cloths are also available in standard package configurations and custom forms. By using these cured silicone insulators, many of the cleaning and coating problems related to silicone grease smear can be avoided (see Figure 5-12).

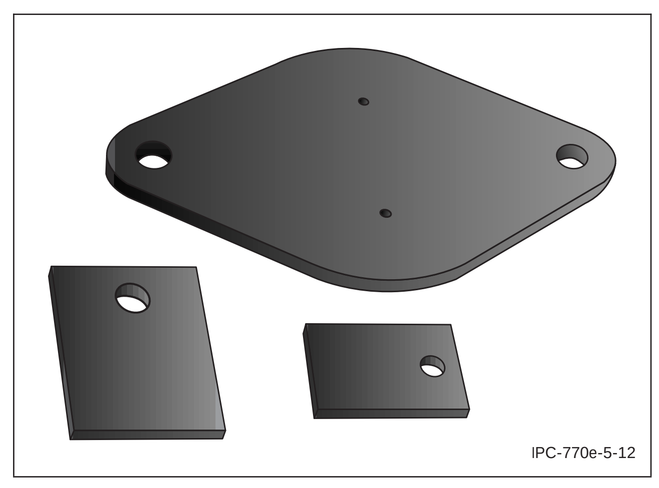


Figure 5-12 Thermally Conductive Insulator

6 ASSEMBLY DESIGN CYCLE

Because of the multistep component mounting operation, the designer of intermixed assemblies must take into account all of the fabrication and assembly steps necessary to complete the electronic assembly. These concerns that take place during the design cycle include:

A. Component Types

- Through Hole
- Leaded SMT
- Leadless SMT

B. Assembly Processes Used

- Single-Sided Assembly
- Double-Sided Assembly
- Component Securing

C. Joining Techniques

- Single-Sided Joining Techniques
- Double-Sided Joining Techniques
- Care Required for Heat-Sensitive Components
- Handling of Unsealed Components

D. Sequence of Events

The last item on the list shown above is usually never considered during the design cycle.

6.1 Types of Assembly Operations Handler capabilities and features vary according to the type of unit and device being accommodated. Automatic units provide throughput rates on the order of 6,000 (and greater) components per hour. Tube adapters are designed to take most tubes currently in use. Automatic assembly machines range from very specific machines that repeat the same task over and over again, to the machines that can be programmed to do several similar processes.

Consideration must be given to complexity, volume of units per run and the product mix to be assembled. Equipment should be selected for high flexibility enabling it to handle a large product mix and short production runs, or chosen for high-speed dedicated equipment that does not allow for much product mix.

The following lists three basic types of equipment available:

- Inline Machines
- Sequential Machines
- Mass Placement Machines

6.1.1 Inline Machines Moderate volume machines that utilize multiple placement heads. These machines can have each head placing a single component or a programmable head that can place a variety of components up to approximately 30,000 components per hour.

6.1.2 Sequential Machines Provide for flexibility of programming placement of components 2,000 to 12,000 per hour. This level of automation allows for some component testing prior to the placement of the board.

6.1.3 Mass Placement Machines Very high volume, fairly dedicated machine used in the matrix of stocks or multiplicity of tapes, which assembles a total circuit with one or more codes of the machine, up to 200,000 components per hour.

6.2 Soldering Operations Either manual or automated. Each of these has several processes.

6.2.1 Manual Soldering Tools and Processes

6.2.1.1 Hot Air Pencils/Heat Guns Both effective and versatile tools for preform soldering. A variety of nozzle shapes are available to localize the heated area. Masks or covers can be used to protect sensitive components. If an inert or reducing atmosphere is required, connecting the intake impeller to a suitable supply of gas can provide this protection.

6.2.1.2 Induction Soldering Confines heating to local areas of a panel or assembly, particularly when unusual shapes or spots are involved. Fast throughput is possible

using coils uniquely designed for reflow of specific areas of interest. Clad coils prevent inadvertent electrical contact with components.

6.2.1.3 Soldering Irons Another effective and versatile tool for performing manual soldering operations. A variety of tip shapes are available to localize the heated area without damaging adjacent parts. Operator skill is required in order to position the solder iron tip at the correct location and to avoid over-heating the joint or plated through hole.

6.2.2 Automated Soldering Processes The following sections describe the specific details of the most common automated processes used for mass production soldering of electronic assemblies.

6.2.2.1 Wave Soldering The large percentage of through-hole board mounted components are mass wave soldered. Small surface mount components such as passive chip capacitors, resistors and SOTs (small outline transistors) are bonded to the bottom side of the board with an adhesive are also wave soldered extensively.

Wave soldering involves the following sequence of operations:

• Fluxing

• Preheating

• Soldering

The wave soldering process includes a pump located in a tank of liquid solder at a temperature of about 235-250°C. This pump generates a positive pressure causing the solder to flow up a chimney or nozzle where it overflows to form a standing solder wave. This solder wave crests higher than the rim of the solder tank, which performs the solder joining of the components to the metallic surfaces on the circuit board.

The preheated assembly receives the balance of the heat required to raise the joint areas to the soldering temperature, causing the liquid solder to wet those areas to be joined.

The assembly is conveyed, usually up a slope, inclined between 4 - 7°, till its bottom surface contacts the crest of the solder wave where the pads, protruding leads, plated holes and bottom-side surface mounted components are soldered.

The solder only wets to, or forms joints on, solderable metallic surfaces. Consequently, no soldering takes place on the board surface that is nonmetallic and poor soldering can occur on any metallic surfaces that are contaminated or have poor solderability. A common wave for soldering traditional boards with leads in through plated holes is the asymmetrical wave used with an inclined conveyor. The majority of the solder flowing from the nozzle flows against the direction of travel of the board. The remaining portion of the solder flows as a smooth laminar stream of solder in the same direction as the board. This small amount of solder flows over a weir, often adjustable in vertical position, so that the speed of the solder flowing towards the exit weir is moving at the same speed as the board and the conveyor. With the board and the solder moving in substantially the same direction and at the same speed, the drainage conditions where the assembly separates from the wave are ideal for optimum soldering results.

Various wave configurations have been used including the narrow parabolic wave, the wide wave, the adjustable wide wave and the hollow jet wave. Some are operated with horizontal conveyors and others with inclined types.

To eliminate solder bridges that sometimes form as a board separates from a solder wave, some wave solder machines may have an air knife fed with hot air to sweep any bridges from the joint areas before the solder has had a chance to freeze. When used in a nitrogen wave soldering system, nitrogen is supplied to the hot knife.

For wave soldering of surface mount assemblies where, in addition to the usual leaded components, small chip components have been glued to the bottom of the board, two solder waves are sometimes used. The first solder wave is usually a high, rather narrow wave made turbulent by some mechanical means. This is achieved by pumping the solder through rows of small, fixed or moving holes at the outlet of the nozzle or by means of a unidirectional hollow jet wave, with its flow trajectory usually aimed in the same direction as the board travel direction. This first turbulent wave is followed by an asymmetrical laminar wave as described above.

The turbulent action of the first wave causes the solder to move in and around all the chip components to help ensure that all solder joints get soldered. Those joints that are still not soldered most probably are soldered when contacting the second wave. In some designs a vibrating device is added to produce additional mechanical pressure in the second laminar wave to promote hole filling and to further help reduce solder skips.

With double wave systems, a separate pump for independent wave height control drives each wave and they are usually found in the same solder pot. Some machines have the two waves in separate solder tanks, in which case, it is possible to control the solder waves at different temperatures.

6.2.2.2 Vapor-Phase Soldering Although each of the above techniques can produce acceptable results, vapor-phase soldering is an extremely consistent soldering process because the soldering temperature is maintained constantly at the boiling point of the primary liquid. Also,

vapor-phase soldering can solder both sides of a printed board structure simultaneously.

The process uses a perfluorinated liquid that is heated to its boiling point, creating a saturated vapor zone. At atmospheric pressure, the temperature of the saturated vapor is the same as the boiling liquid. Typically, a perfluorinated fluid with a working temperature of 215°C is used for eutectic grade solder. Fluids with other boiling temperatures are available for lower or higher solder compositions, in multistep soldering, or for use with pure tin.

The soldering process moves the populated printed board structure into the vapor zone using either a vertically operating baton system or a conveyorized in-line system. In either configuration, reflow cycle times of 30 to 60 seconds are common.

The printed board structures come out of the soldering process uniformly soldered and dry. The uniformity results from the inert, oxygen-free conditions in the vapor and the precise maximum temperature limitations of the process.

6.2.2.3 Conduction-Reflow Belt Soldering A conduction-reflow belt system uses conduction to transfer heat through the printed board structure. This is accomplished by a series of heated platens located under a continuously moving belt.

The platen temperature and belt speed is individually controlled so that the reflow profile can be varied for different types of printed board structures, which may have different melting temperatures. Since heat is conducted through the board, a thermal gradient exists across the printed board structure. Increasing or decreasing the flow of air over the belt as the assemblies travel off the end of the final platen can also vary the cooling rate.

Because the conduction of the heat through the printed board structure depends on the contact of the structure to the belt, a weighted fixture is usually used to apply pressure to multiple points on the structure. This pressure is applied from the primary side of the printed board structure and is designed not to interfere with the chip carriers on that side. Universal fixtures are usually designed for multiple printed board structures.

A typical schedule for a three-stage conduction reflow soldering belt system is as follows:

1st platen:	50°C
2nd platen:	200°C
3rd platen:	230°C
Belt speed:	10-11 IPS
Air flow:	As required

The belt speed should be adjusted to allow the solder to reflow for a total of 30 to 60 seconds. In addition, the airflow should be adjusted so that the solder, when solidified, is shiny and not grayish in color.

6.2.2.4 Reflow Oven Electrically heated air circulation ovens are suitable for batch operations, provided the whole assembly can withstand the soldering temperature. Inert or reducing atmospheres can be used if necessary. For continuous operation, gas or electrical conveyorized furnaces may be used and these can also allow the use of controlled atmospheres. Smaller units require careful matching of temperature settings with a thermal pad of product if close control of temperature profiles is required.

6.2.2.5 Heater Bar Reflow Soldering Attaches leaded surface mount devices to printed board conductive land areas. Heat is supplied via electrical resistance heating of the heater bar tip. The tip temperature is controlled by a variable current feedback loop with a thermocouple on the heat bar tip.

The Pulsed Heat Cycle can be either pulsed or constant. The pulsed heat cycle system consists of the following steps:

1. Heater bars are aligned over leads to be soldered.
2. Heater bars descend on top of the leads exerting approximately 0.1 to 0.2 pounds per lead being soldered.
3. Power supplies preset for time at temperature are activated and send variable current to the heater bar tips to reflow solder the leads to the printed board structure.
4. After the soldering cycle time at temperature is completed, the power supplies are deactivated and air jets, directed at the heater bars, are activated. Meanwhile, the heater bars maintain their contact pressure on the leads for a specified dwell time allowing the leads to cool undisturbed.
5. After the solder has solidified, the heater bars are retracted and aligned over the next set of leads to be reflow soldered.

The Constant Heat Cycle consists of the following steps:

1. Heater bar tips are heated to and maintained at a predetermined temperature setting.
2. Heater bars then contact the leads for a specified amount of time, reflow soldering the leads.
3. The heater bars are then removed allowing the joints to cool undisturbed.
4. Both methods have different applications but require the common set up of tinned leads and a predetermined amount of solder paste on the conductive land area.
5. When using a pulsed heat cycle system, take care to properly form the leads. Otherwise, the pressure of the heater bars induces mechanical stress into the joints because the leads are forcibly held in place during cooling. This can cause solder joints to crack during burn-in, thermal and vibration cycling.

6.2.2.6 Infra-Red Soldering Unfocused infra-red lamps can rapidly heat the printed board structures to soldering temperatures, although features such as component color and surface texture influence the rate of heating and the final temperature. Polished aluminum reflectors may be used to minimize local heating. Focused infra-red heating provides an efficient means of even more rapid heating, provided the distribution of preforms lends itself to localized patterns of heating. A throughput of 2 m/min or more is possible.

6.2.2.7 Laser Reflow Soldering This process uses a laser beam to supply the heat necessary for reflow soldering. Presently, the continuous wave and YAG laser is preferred, although some companies have demonstrated success utilizing a carbon dioxide or eximer laser. This is a noncontact process unless tooling specifically designed to apply pressure is used.

Other advantages of this process are the extremely fast soldering and localized heat cycles. A typical joint is reflowed in less than one second. This reduces the amount of heat conducted away and therefore localizes the heat applied to the solder joint area.

Both leaded and leadless components can be reflowed with this process. It is recommended that when reflow soldering leadless components, the laser beam should be oriented at approximately 45° to the soldering and directed at the solder to solder interface. A leaded device, where the beam is oriented at 90° to the solder surface, is directed at the component lead.

The reflow soldering process typically involves mounting the populated printed board structure to a computer controlled motion system that loads a computer program which automatically directs the laser to each joint and controls the power level and time duration of the laser at each joint. This verifies the initial joint location, usually with a closed circuit TV system or a He-Ne spotting laser, placing the system into the automatic mode, thus allowing the system to reflow solder all programmed joints.

A laser soldering system properly set up and programmed yields highly consistent solder joints. However, consistent processing (i.e., lead forming, lead tinning, amount of solder on the land, and component mounting) before reflow soldering is an integral part of this process and requires strict controls.

6.3 Assembly Sequence

6.3.1 Inspect Before Assembly Each printed board structure and its components should be examined to ascertain that no damage has been incurred during transit or handling, and that component mounting is in accordance with the appropriate requirements.

6.3.2 Substrate Preparation Printed boards should be tested for solderability before assembly. If solderability is not acceptable, then pretreatment prior to assembly may be required to enhance solderability and subsequent quality of the soldered assembly. Solder masking may or may not be present dependent on specifications. Typical pretreatment are degreasing (surface contamination, e.g., dirt, oils), brightening (chemical activation of solder and/or copper), and baking (moisture). Baking of the substrate may be necessary in order to prevent delamination of the substrate.

6.3.3 Component Preparation (Tinning/Solder Dipping) Component leads not meeting the designated solderability requirements may possibly be reworked by tinning/solder dipping, prior to soldering. All portions of the wires or leads that come in contact with the area to be soldered must be solderable. Baking of moisture sensitive components may be necessary.

6.3.4 Assembly Process Sequence Assembly processes for production of printed board assemblies differs according to the type of product (e.g., through board, surface mount, mixed technology or chip on board), and within types according to company expertise, experience and preference.

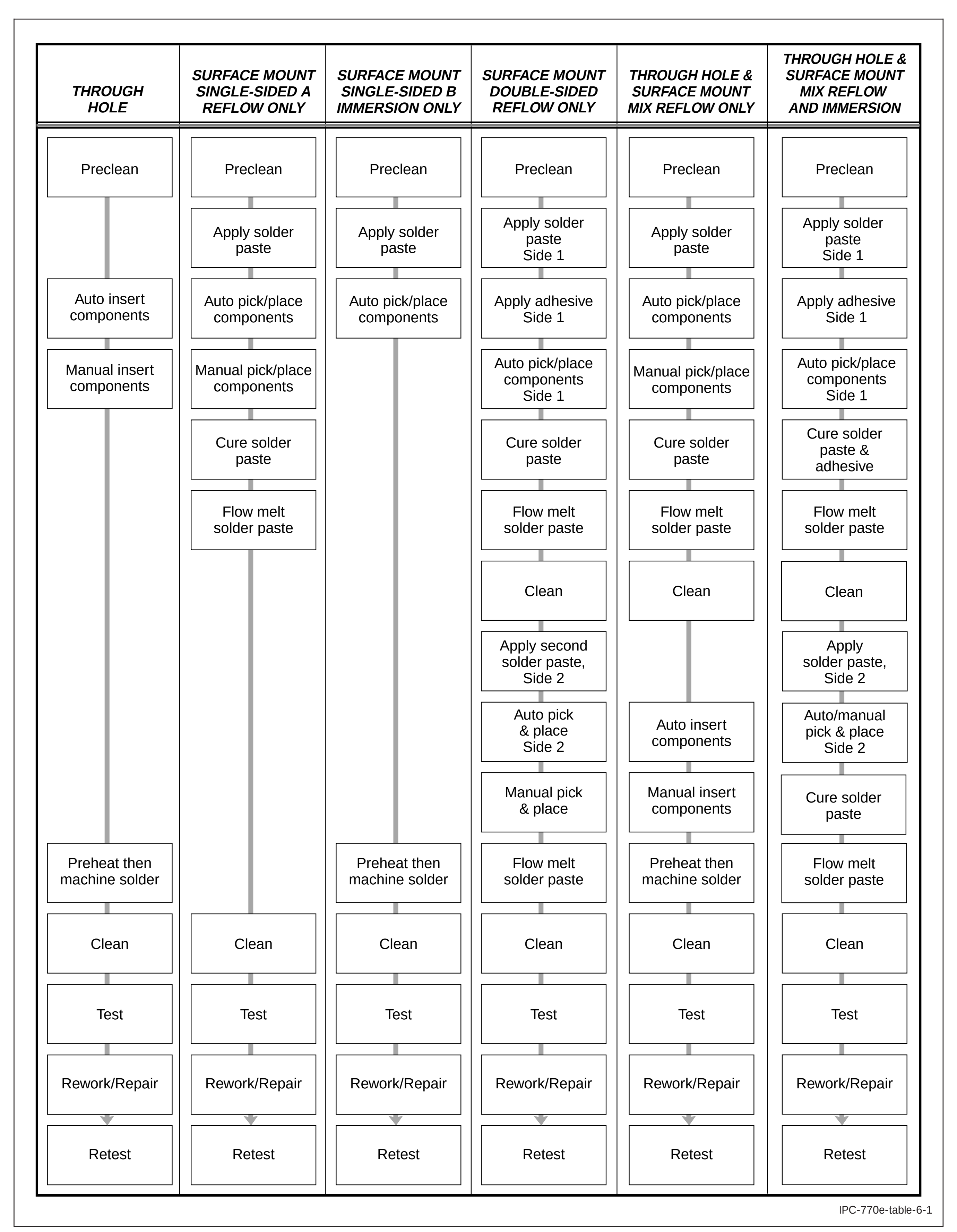
The manufacturing engineer usually establishes the process sequence for a particular line to act as a planning aid, an equipment requirement guide, a manpower requirement guide, and a list of the necessary process steps. However, it is important that comparative process options such as those shown in Table 6-1 are available at the design stage if the full benefits of each process sequence are to be realized. For example, designers should be aware that the assembly process for a double-sided or a mixed technology PWB would be more complex than for a single-sided PWB. Such a comparison also allows equipment cost and space comparisons, and pinpoints necessary material changes.

Other decisions such as the choice of individual machine or equipment processes may be based on component temperature sensitivity, cleanliness requirements, component marking stability, and component bond robustness. Ultimately, all considerations are combined in selecting an assembly process.

Table 6-1 shows the characteristics of different surface mount and through-hole assembly variations.

6.4 Mass Attachment Properties

6.4.1 Machine Soldering Processes Soldering is defined as a joining process with the use of heat (below 400°C) and a nonferrous filler metal that has a melting temperature below that of the base metals to be joined.



THROUGH HOLE	SURFACE MOUNT SINGLE-SIDED A REFLOW ONLY	SURFACE MOUNT SINGLE-SIDED B IMMERSION ONLY	SURFACE MOUNT DOUBLE-SIDED REFLOW ONLY	THROUGH HOLE & SURFACE MOUNT MIX REFLOW ONLY	THROUGH HOLE & SURFACE MOUNT MIX REFLOW AND IMMERSION
Preclean	Preclean	Preclean	Preclean	Preclean	Preclean
	Apply solder paste	Apply solder paste	Apply solder paste Side 1	Apply solder paste	Apply solder paste Side 1
Auto insert components	Auto pick/place components	Auto pick/place components	Apply adhesive Side 1	Auto pick/place components	Apply adhesive Side 1
Manual insert components	Manual pick/place components		Auto pick/place components Side 1	Manual pick/place components	Auto pick/place components Side 1
	Cure solder paste		Cure solder paste	Cure solder paste	Cure solder paste & adhesive
	Flow melt solder paste		Flow melt solder paste	Flow melt solder paste	Flow melt solder paste
			Clean	Clean	Clean
			Apply second solder paste, Side 2		Apply solder paste, Side 2
			Auto pick & place Side 2	Auto insert components	Auto/manual pick & place Side 2
			Manual pick & place	Manual insert components	Cure solder paste
Preheat then machine solder		Preheat then machine solder	Flow melt solder paste	Preheat then machine solder	Flow melt solder paste
Clean	Clean	Clean	Clean	Clean	Clean
Test	Test	Test	Test	Test	Test
Rework/Repair	Rework/Repair	Rework/Repair	Rework/Repair	Rework/Repair	Rework/Repair
Retest	Retest	Retest	Retest	Retest	Retest

IPC-770e-table-6-1

Table 6-1 Through Hole and Surface Mount Assembly Process Flow Comparison

Soldering is a practical technique for producing mechanically sound and electrically reliable interconnections. Different soldering processes exist, suited for a variety of electronics assembly applications and technologies. The following sections describe the specific details of the most common processes used for mass production soldering of electronics assemblies.

6.5 Environment (Nitrogen)

6.5.1 Controlled Atmosphere Soldering A great deal of investigation has been focused on the potential benefits of using an inert gas in the mass soldering processes. Research has focused on reactive and protective atmosphere systems. Reactive atmospheres utilize gases that react with the surfaces to be soldered and the solder source resulting in a clean, solderable surface. Protective atmospheres displace the oxygen in the soldering zone of the mass soldering processes thus allowing the fluxes to remove the surface oxides without reoxidation.

The majority of the controlled atmosphere soldering systems on the market use protective gases. Nitrogen is the most prevalent gas used. An oxygen concentration less than 100 ppm has been found to provide excellent soldering results. Nitrogen consumption varies depending on the length of machine, soldering workload, and type of entry/exit interlock system employed. The use of controlled atmosphere soldering systems can produce the following benefits:

- Improved Soldering Yield
- Reduced Flux Consumption
- Improved Solder Joint Appearance
- Improved Solder Joint Geometry
- Improved Flux Residue Removal
- Reduced Machine Maintenance

7 PLACEMENT GUIDELINES

Pick and place equipment requires ‘‘keep-out’’ areas for essential equipment clearances. The placement and spacing of components is critical for manufacturing assembly and inspection, component removal, cleaning, thermal heat management, and test probe access.

7.1 Placement Technology

7.1.1 Placement During assembly sequencing, singular component placement (one component at a time) and multiple component placement are two major items to consider. The primary concerns in these areas are the tool head clearances for automatic placement and the setup procedures that are necessary in order to ensure that the placement of one component does not dislodge or disturb the placement of a previously set part.

In addition, the type of board or packaging interconnection structure used to interconnect the components can also play a dramatic role in the sequencing of electronic component mounting. Examples of eight basic construction formats applicable to this specification are shown in Figures 7-1 through 7-6, together with typical associated process sequences.

7.1.2 Process Identification

7.1.2.1 Construction Formats and Process Sequences Figures 7-1 through 7-6 show examples of six basic construction formats applicable to this specification, together with typical associated process sequences.

Note: Where manual insertion and soldering of leaded components is required after a mass immersion soldering operation, covering the related plated through-holes with a peelable resist to prevent them being filled with solder may be necessary.

Looking at the intermixed assemblies, components that are mounted through hole are usually positioned on one side; whereas components mounted on the underside of the board are usually those of the surface mounted variety. In this technique, the surface mounted components are usually attached to the board using an appropriate adhesive. The through hole components are then automatically inserted, and the entire assembly is passed through a solder wave.

Some assemblies may require some through-hole components (usually connectors) to be mounted on both sides of the board. This assembly process may require additional soldering processes such as partial wave soldering, solder fountain, paste in hole, and solder preforms and/or hand soldering of these parts.

The technique for the assembly operation can vary, depending on the type of component, the number of different components being mounted, and the mounting techniques themselves. If a single part is surface mounted amidst a large variety of through-the-board mounted components, the surface mounted part becomes a minor part of the assembly operation. The same holds true if the through-the-board parts are in the minority. In these instances, manual or semiautomated techniques are usually employed, especially if the total quantities of assemblies do not justify the set up time required for automated component mounting.

When there is an equal number of through-the-board and surface mounted components, the tooling concept for automated component mounting must consider the need for special fixturing or attachment techniques.

Double-sided or multilayer printed board structures have similar characteristics for the mounting of parts. Major differences between the single-sided board and double-sided/

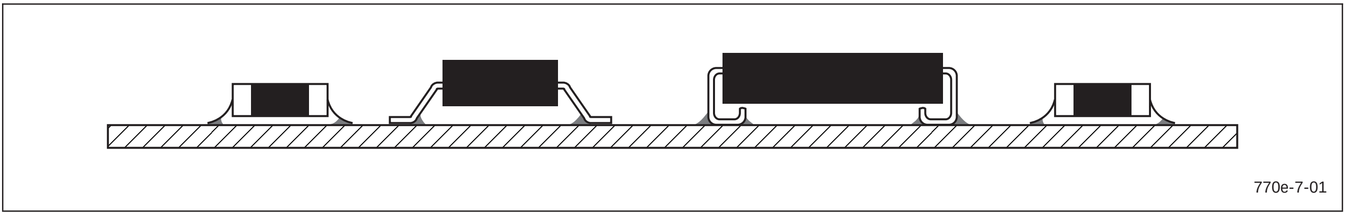


Figure 7-1 Single-Sided Surface Mount Assembly, Reflow Only (See Table 6-1 SURFACE MOUNT SINGLE-SIDED A REFLOW ONLY)

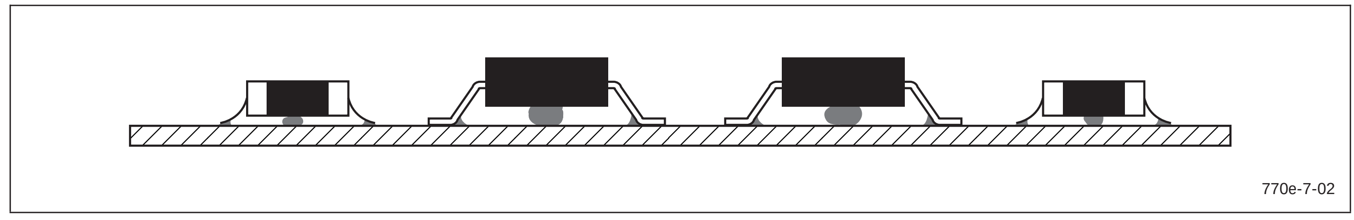


Figure 7-2 Single-Sided Surface Mount Assembly, Immersion Only (See Table 6-1 SURFACE MOUNT SINGLE-SIDED B IMMERSION ONLY)

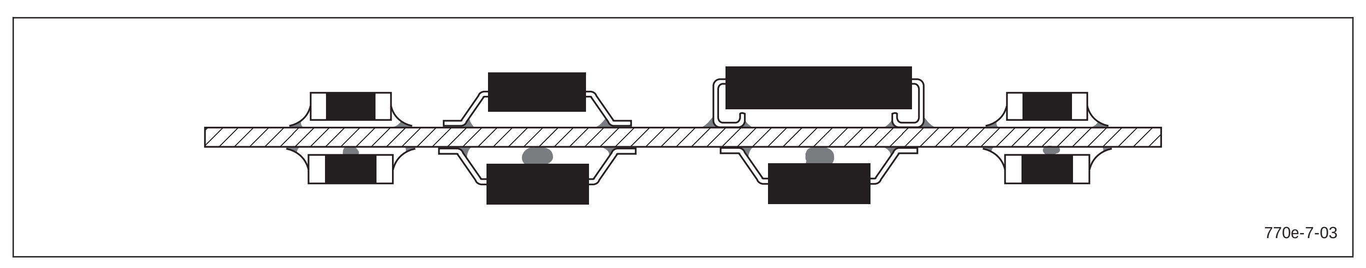


Figure 7-3 Mixed Technology Assembly, Double-Sided, Reflow Only (See Table 6-1 SURFACE MOUNT DOUBLE-SIDED REFLOW ONLY)

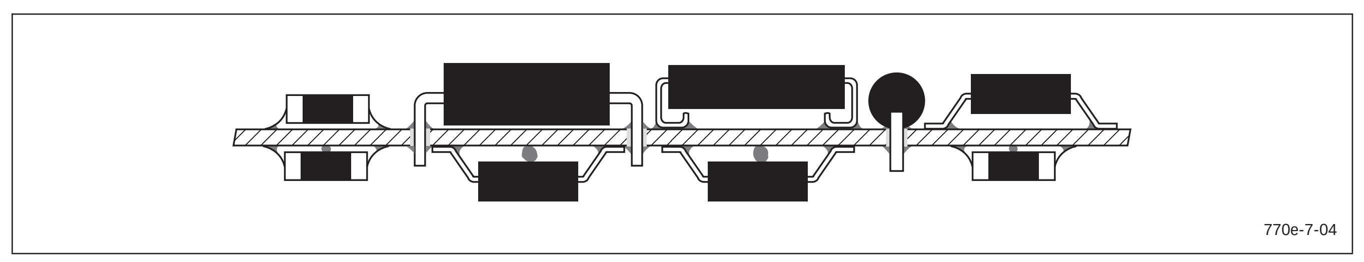


Figure 7-4 Mixed Technology Assembly, Double-Sided: Reflow and Immersion (See Table 6-1 THROUGH HOLE AND SURFACE MOUNT MIX REFLOW AND IMMERSION)

multilayer assembly are that leads of through hole components are usually in plated-through-holes. The tolerances of plated-through-holes must be more liberal to allow for the plating build-up; therefore, the component mounting process is sometimes more restricted, based on the manufacturing allowances incorporated into the plated-through-hole printed board. The attachment techniques for through hole components are usually some form of wave soldering.

When parts are surface mounted to double-sided or multilayer printed boards, the surface mounted parts may be mounted all on one side or both. The attachment techniques for surface mounted boards are usually some form of reflow soldering.

7.1.2.2 Manual Assembly Manual techniques in an intermixed assembly play an increased role due to the necessity for secondary component placement and attachment operations. Lack of automated assembly head clearances, special part types, heat sensitive parts, or unsealed parts all require special handling and are, therefore, prime candidates for manual component mounting techniques.

With the ever-increasing trend toward miniaturization, the manual techniques usually require magnification and special tool dexterity in order to insure that small parts are properly mounted, placed or positioned. Special equipment is available that provides a semiautomated technique of taking one component at a time and positioning it by having the machine assist the operator through special enhanced movement. Even with manual or semiautomated techniques, design should provide for adequate clearance around components, so that placement heads or tools do not interfere with previously placed components.

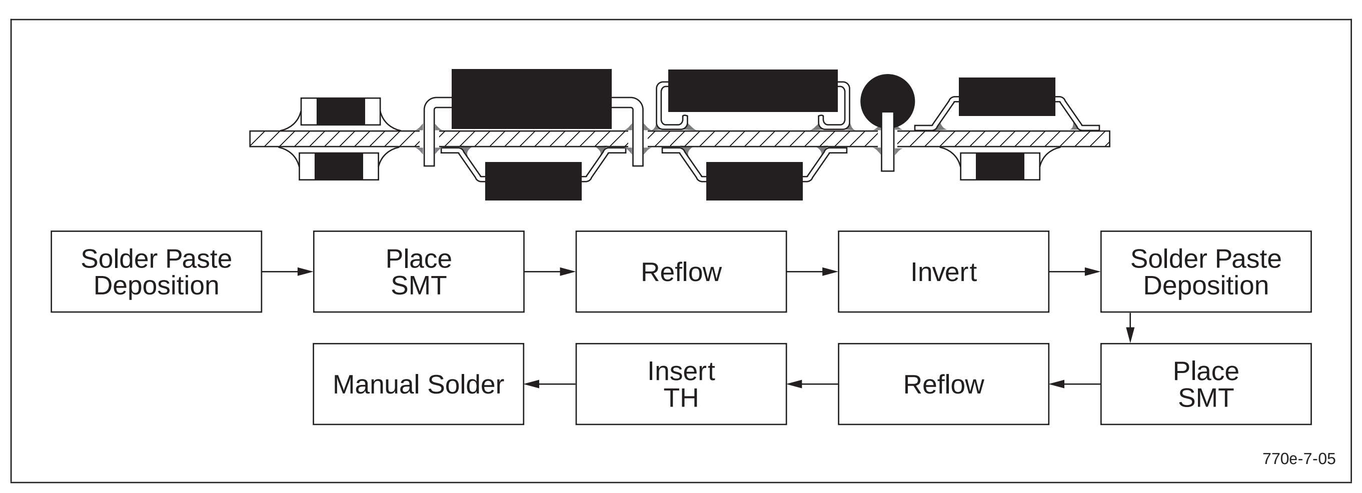


Figure 7-5 Mixed Technology Assembly, Double-Sided Reflow and Manual

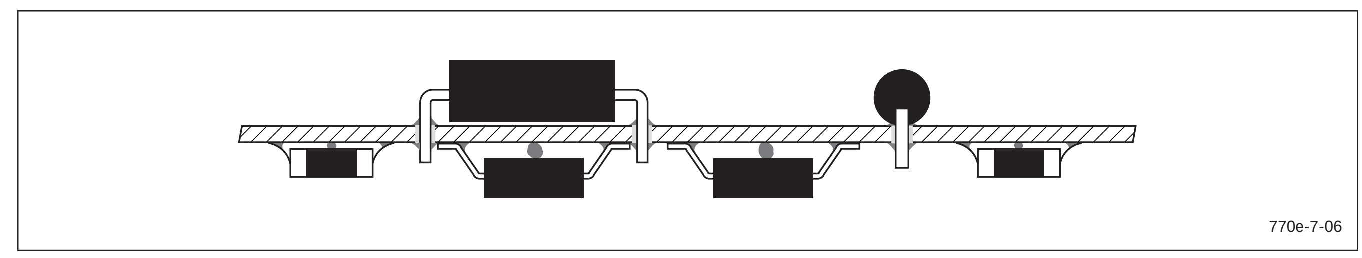


Figure 7-6 Mixed Technology Assembly, Double-Sided, Immersion Only

7.1.2.3 Automated Assembly Automated techniques used for intermixing of components are similar to those used for boards that have only through hole mounted or only surface mounted components. Major considerations are given in automated techniques for special fixturing, which reduce shock and provide clearance for components that have previously been mounted.

Because of the special cost of tooling and set up time of intermix printed board assemblies, many designs are assembled in panel form rather than in individual board form. This is especially helpful when a manufacturer can set up his equipment for a standard size panel and the equipment is, therefore, impervious to the fact that the panel contains one or many boards.

Panel assembly requires special tooling and registration incorporated into the panel during the manufacturing operation. Tooling holes are located as shown in Figure 7-7. These require special close tolerance considerations to insure that the automated equipment is able to locate and position components.

Some assembly equipment uses special sensing symbols that have been incorporated into the design. The equipment senses the location of the symbol and can zero in on a particular board, or even pattern. The assembly equipment can then compensate for material movement or shifting of patterns. With special tooling, features, or holes, the automated assembly can, therefore, accommodate panels of 467.2 mm [18 in] to 609.6 mm [24 in] without any loss of accuracy of the component placement task (see Figure 7-8).

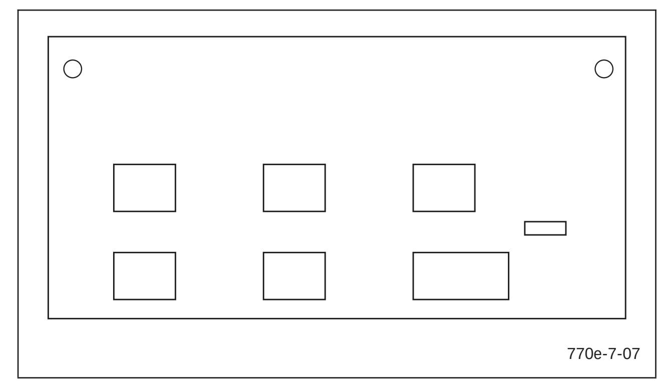


Figure 7-7 Panel Assembly Tooling Holes

Designs should consider whether the assembly is accomplished using board assembly or panel assembly. Board to component orientation is critical in some instances where the parts pass through the wave and are, thus, attached to the land patterns. Placement of parts and orientation of parts are critical to insure that the part body does not shadow the solder joint. The orientation of the component boards on the panel plays a significant role in the type of solder joint when the boards are to be wave soldered.

7.2 Design Checks

Applies to each individual board design and includes the following checking activities

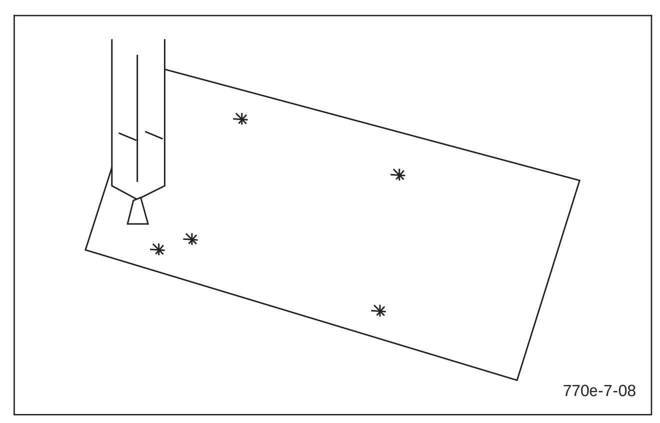


Figure 7-8 Panel Assembly Tooling Holes

necessary to assure satisfactory mechanized equipment performance and manual workmanship. The list of checks is not intended to be exhaustive and does not include all reliability aspects.

7.2.1 Design Checks for All Assembly Types Check that:

- The board design conforms to applicable layout component clearance and orientation rules for the intended soldering and assembly processes.
- Permits specified for post-assembly component positioning and relevant solder joint contour requirements given in the J-STD-001, IPC-A-610 or equivalent are met.
- Sufficient space free of components has been allowed for a supporting carrier to prevent sagging when the board is to be wave or drag-soldered and supports components needing preheating to within 100°C (or less) of the solder bath temperature (e.g., leadless multilayer ceramic capacitors).
- All land layouts and associated tracks provide thermal isolation against connected large thermal masses so that manual soldering and rework can be carried out with minimum time-temperature combination.
- The printed board and its specified dimensions, flatness, coatings, resists and components are suitable for use through the intended processes and process equipment without degradation of reliability of the assembly (if in doubt, seek the supplier's written confirmation).
- The distribution of copper layers and earth-plane design are balanced to achieve the best possible board flatness after soldering. Wherever practicable, large copper areas (e.g., ground planes, power planes) should be cross-hatched to reduce delamination risks.
- Sufficient clearance is available around each component to permit the use of the appropriate manufacturer's recommended rework tool and method.
- All ''in circuit'' or other test probes can contact the board without touching any solder joints, component leads or bodies.
- Available in-circuit test equipment has sufficient nodes to meet the test requirement on the basis of checking all required components - preferably in one pass through the equipment.
- Within the constraints of available knowledge, legal safety requirements and relevant national or international safety standard specifications, the proposed design is reasonably safe when used in the manner and environment for which it has been designed.

A hazard and risk analysis is helpful in assessing this issue and is mandatory in some applications. Where necessary, appropriate warnings to users should be made available.

7.2.2 Design Checks for Surface Mounted Assemblies

Check that:

- All design checks stated in 7.2.1 apply.
- The layout enables the planned solder paste or adhesive deposition equipment to perform at acceptable speed and quality.
- When mass reflow soldering is intended, land patterns for small 2, 3 and 4 termination/lead components have balanced thermal mass and balanced surface tension effects to avoid unwanted movement during soldering.
- The layout allows sufficient clearance for surface mount component placement, pre and post-soldering visual inspection of component bodies and solder joints and electrical probe testing of the assembly during in-circuit and/or functional test.
- Solder joints to surface mounted components are sufficiently spaced away from break lines when individual circuits are separated (break-out) from a step and repeat array panel.
- Test probe pads are spaced to allow use of robust, reliable test probes, e.g., not less than 2.5 mm apart (ensure that the requirements of 17 are met).
- The designed test circuitry and supporting test jig(s) does not harm the assembly function or structure.
- Excessive voltages are avoided.
- Mechanical forces from test probes do not distort boards after soldering even bowed, twisted or dished boards.
- Sufficient land length is available when leadless multilayer ceramic capacitors are used.
- The characteristics of the fiducial marks (e.g., size, shape, surface finish, contrast, etc.) used on the board are suitable for the machines involved, e.g., as to their size, shape, surface finish, contrast when optical alignment is intended on printing or automatic component placement machines.

7.2.3 Design Checks for Mixed Technology Assemblies Involving Auto-Placement and Auto-Insertion Check that:

- The design checks stated in 7.2.1 and 7.2.2 apply.
- Sufficient clearance is available around surface-mounted components to avoid damaging them during subsequent through-hole insertion and crop and clinch operations.

7.3 Specification and Procurement of Components To assist in assuring that components supplied are 'fit for purpose' and enable rework to be kept to a minimum, the following workmanship requirement should be implemented:

- Product Processes and Applications
- Component Package Style
- Component Transit Packaging
- Date of Manufacture and Solderable Coating Thickness

7.3.1 Product Processes and Applications The procuring authority should, in advance of contract placement and purchase, advise the assembler of the application field of the product and its related environmental and mechanical test specifications. The assembler should pass this information on to suppliers and also inform them of the intended assembly process and the relevant time-temperature cycles and cleaning methods to be seen by the components. This includes rework of solder joints and any subsequent soldering operation required for populating both faces.

7.3.2 Component Package Style The assembler should ensure that the components are specified to arrive in the package style for which the board layout has been designed. The assembler should also ensure that the packaging format can handle the appropriate sequencing/insertion or placement equipment, e.g., in tapes, reels, tubes, trays and bulk feed magazines.

7.3.3 Component Transit Packaging To optimize the maintenance of solderability, the transit packaging of solderable components should be specified as maintaining a low relative humidity and protecting against atmospheric contamination in transit and in any intermediary storage, e.g., on a distributor's premises. Contact between termination materials/lead surfaces and soft plastic materials, such as polyethylene, cling film, transit or storage of reels, tubes or magazines, packed or unsealed in hygroscopic box materials such as cardboard, should be avoided wherever practicable.

In particular, packaging for ceramic and other small components should not permit jostling and abrasion of loose components.

7.3.4 Date of Manufacture and Solderable Coating Thickness Where necessary, the assembler should ascertain the date of manufacture of components and the guaranteed minimum solderable coating thickness and method of applying it. This information assists in determining their suitability for high post-soldering yield.

The recommended minimum solder coating thickness on any one lead is 6 µm for components to be used within 12 months of manufacture and 8 µm for any longer time. Coatings other than solder may require different minimum thickness.

7.4 Specification and Procurement of Printed Boards To assist in assuring that substrates/printed boards supplied are ''fit for purpose'' and enable rework to be kept to a minimum, the following workmanship guidelines should be implemented:

- Specifying Printed Boards
- Notifying Assemblers and Their Suppliers
- Suitability for High Assembly Yield

7.4.1 Specifying Printed Boards Dimensional and accuracy data for board size, conductor tracks, pad, lands and hole specifications should be defined (particularly fine tracks). Solder coating type and thickness range, applicable optical recognition mark shapes, sizes, positions, and surface finish; resist type, thickness and alignment accuracy; applicable protective surface finishes, break-out dimensional requirements (e.g., lug widths and positions, slots, scribe lines) and the required bare board flatness should be referred to IPC-6010 Series.

7.4.2 Notifying Assemblers and Their Suppliers Before procurement, the end-user should advise the manufacturer of the application or classification level of the product and its related environmental and mechanical test specifications. The manufacturer should pass this information on to suppliers. The manufacturer should also inform them of the intended assembly process, the relevant time-temperature cycles and cleaning methods to be seen by the substrate or board. This includes rework of solder joints and any subsequent soldering process required for populating both faces.

7.4.3 Suitability for High Assembly Yield To assist in assuring that substrates/boards arrive in a suitable condition for giving high-yield in placement and soldering operations:

- The manufacturer should ensure that the land surface finish and solderability specifications applied by suppliers to their products are suitable for the applicable method(s) of placement and soldering.
- The method of applying the solderable coating, the solder coating flatness and thickness range (if the finish is solder), and for optical sensing, the optical characteristics of the surface, are relevant parameters.
- The useful storage life of anti-oxidant and preflux coatings should not be exceeded (Refer to 7.4 (d)).

• The manufacturer and supplier should agree on the transit packaging materials and the maximum stack quantity. This should be specified as part of the contract (hygroscopic materials or those having significant free sodium, chlorine or sulfur ion content (e.g., shrink film, cling film) should not be allowed in contact with solderable surfaces).

7.5 Specifications and Procurement of Process Materials

7.5.1 Solder Pastes and Adhesives To assist in assuring that materials arrive in a suitable condition for giving high yield in reflow soldering operations, the specification should require the supplier to state the date and country of manufacture of the paste or adhesive. The supplier should be required to provide the key to interpreting this data.

To minimize the exposure to air of solder paste intended for printing and hence reduce the risk of solder balling, procurement should preferably be based on a paste container size that is used up within 36 hours of opening and having a resealable lid.

Dispensing syringes, though sealed in light proof material for transit and storage, should preferably be transparent so that any signs of separation between the paste carrier and the solder particles can be seen.

7.5.2 Solder Preforms The assembly sequence using preforms can be very simple. The placement method of the preforms between component parts or component and substrate is often the single most unique feature of a preform process. The preform materials should be fixed or located between the components of the joint with sufficient accuracy to insure that upon melting the metal contacts, both parts of the joint so that they wet and surface tension forces can act to draw them into perfect alignment. Finally, the preform must be reflow melted. Solder preforms may be located by placing them over a lead or projection in the chip carrier, or by positioning them in a groove or notch on the substrate. Another alternative is to use auxiliary jigs and plates to immobilize preforms until the reflow operation. Regardless of the placement method, the preforms may be handled through simple manual transfer, vibrator units, tumble plates, or two part alignment plates.

In general, flux cannot be used to tack preforms in place since the flux layer melts before the metal, allowing the solid preform to float and move over the substrate. The same applies to using partial flux reflow from flux filled and flux-coated preforms.

Metal-coated preforms, however, can be affixed by partial reflow, provided there is sufficient difference in melting point between the cladding alloy and the core. Reflow of the cladding layer can be used to attach the preform to one side of the joint, which can then be fully assembled and reflowed at the higher temperature to complete the bonding operation.

8 INTERCONNECT TECHNOLOGY

The printed board design principles recommended in this standard consider current test and manufacturing capabilities. Exceeding the limitation of these capabilities requires concurrence of all participants in the process including manufacturing, engineering and test technology. Involving test and manufacturing early in the design helps to move a quality product quickly into production.

Manufacturing engineering should be consulted regarding any components outside the scope of this document.

8.1 Component Spacing

8.1.1 Component Considerations The land pattern design and component spacing affect the reliability, manufacturability, testability and reparability of surface mount assemblies. A minimum inter-package spacing is required to satisfy all these manufacturing requirements. Maximum inter-package spacing is limited by several factors, such as, available board space, equipment weight considerations, and circuit operating speed requirements. Some designs require that surface mount components be positioned as close as possible.

8.1.2 Wave Solder Component Orientation On any printed board assembly where a side is to be wave soldered, the preferred orientation of devices on that side is as shown in Figure 8-1. The preferred orientation illustrated is used in order to optimize the resulting solder joint quality as the assembly exits the solder wave. All polarized surface mount components should be placed in the same orientation, when possible. The following additional conditions should be considered for optimum solderability:

• All passive components should be parallel to each other.

• The longer axis of SOICs and the longer axis of passive components should be perpendicular to each other.

• The long axis of passive components should be perpendicular to the direction of travel of the board along the conveyer of the wave solder machine.

8.1.3 Component Placement Similar types of components should be aligned on the board in the same orientation for ease of component placement, inspection, and soldering. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance guidelines ultimately driving the placements. In memory boards, for example, all of the memory chips are placed in a clearly defined matrix with pin one orientation in the same direction for all components. This is a good design practice to carry out on logic

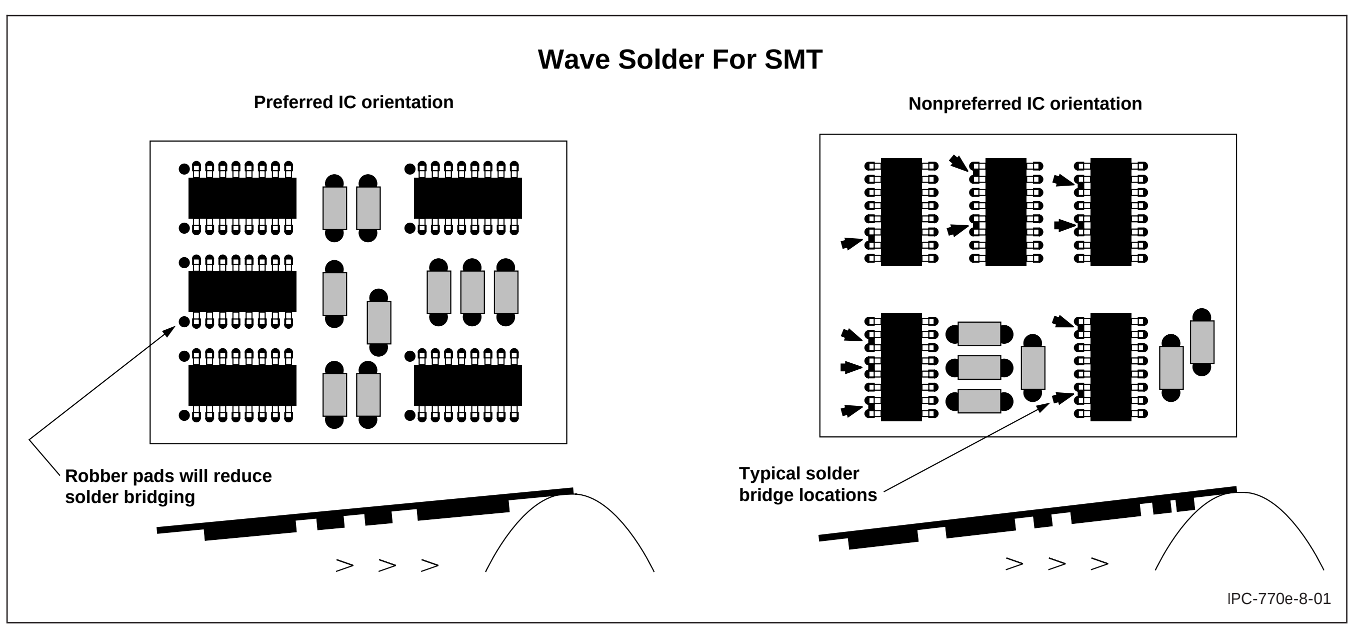


Figure 8-1 Component Orientation for Wave-Solder Applications

designs where there are many similar component types with different logic functions in each package. On the other hand, analog designs often require a large variety of component types making it understandably difficult to group similar components together. Regardless of whether the design is memory, general logic or analog, it is recommended that the orientation of pin 1 on all IC components be the same, provided that product performance or function is not compromised.

8.1.4 Grid-Based Component Positioning Surface Mount Technology component placement is generally more complex than Through Hole Technology printed boards for two reasons: higher component densities and the ability to put components on both sides of the board. In high-density SMT designs, however, the spacing between lands is often less, down to 0.20 mm. Grid-based device placement is complicated by the large variety of component shapes associated with the SMT component packages.

Two effects created by random component placement are a loss of uniform grid-based test node accessibility and a loss of logical, predictable routing channels on all layers (possibly driving layer counts). In addition, the accepted international grid identified in IPC-1902 states that for new designs the grid should be 0.5 mm, with a further subdivision being 0.05 mm. One solution to the problem is to build CAD libraries with all component lands connected to vias on 0.05 mm centers (or greater, based on design) to be used for testing, routing, and rework ports. Then, when placing the component on the CAD system, make sure that there is a minimum space of 0.5 mm between lands. Next, snap the vias of the component being placed out to the next 1.0 mm grid point. With this procedure, all of the components should have between 0.4 mm and 0.6 mm (or an average of 0.5 mm) spacing between the lands. From the assembly point of view, it is easier to process a printed board (PB), which has uniform component center-point spacing across the board in both directions (see Figure 8-2).

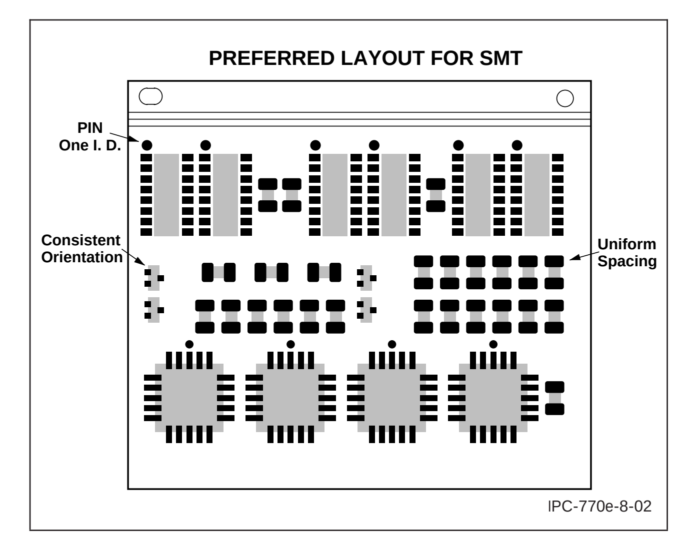


Figure 8-2 Alignment of Similar Components

8.2 Single and Double-Sided Board Assembly The term single-sided refers to components mounted on one side, and the term double-sided refers to components mounted on both sides of the board. Designers should concentrate on locating all components on the primary side of the board whenever possible without creating component spacing violations. This may result in a lower assembly cost. Double-sided boards, using conventional SMT design rules, may require double-sided (or ‘‘clamshell’’) test fixtures, increasing the cost of the test fixtures.

8.3 Component Standoff Height for Cleaning The recommended minimum component standoff height for

cleaning is affected by the distance across the diagonal of the component lead pitch.

If a minimum standoff cannot be achieved, proper cleaning under the component may not be possible. In this case, it is recommended that a no-clean flux is used and/or resist material should be retained over all exposed via and circuit patterns located under devices.

8.4 Fiducial Marks A fiducial mark is a printed artwork feature that is created in the same process as the circuit artwork for optical recognition systems. The fiducial and a circuit pattern artwork must be etched in the same step.

The fiducial marks provide common datum points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of fiducial marks.

8.4.1 Global Fiducials Global fiducial marks are used to locate the position of all circuit features on an individual board. When a multi-image circuit is processed in panel form, the global fiducials are referred to as panel fiducials when present for the panel (see Figure 8-3).

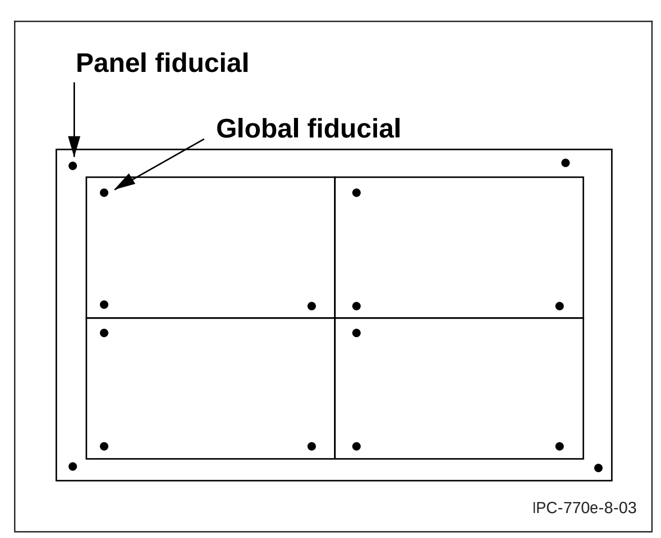


Figure 8-3 Panel/Global Fiducials

8.4.2 Local Fiducials Local fiducial marks are used to locate the position of an individual component requiring more precise placement (see Figure 8-4).

A minimum of two global fiducial marks is required for correction of translational offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposite and as far apart as possible on the circuit or panel.

A minimum of three fiducial marks is required for correction of nonlinear distortions (scaling, stretch and twist). These should be located as far apart as possible in a triangular position on the circuit or panel.

A minimum of two local fiducial marks is required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within the perimeter of the land pattern.

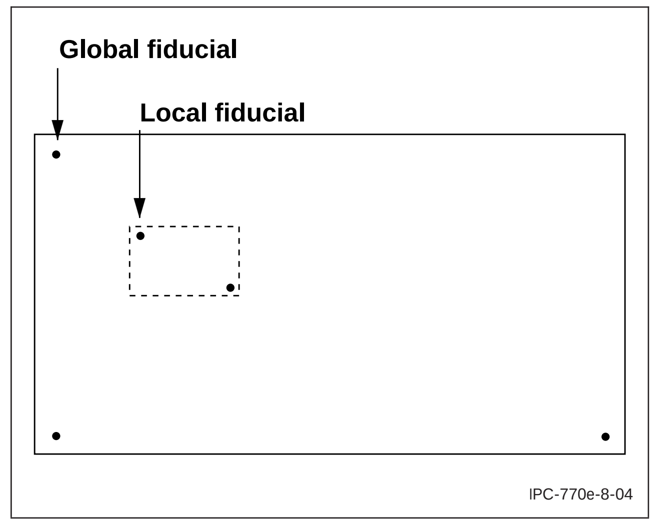


Figure 8-4 Local and Global Fiducials

It is good design practice to locate global or panel fiducials in a three-point grid-based datum system as shown in Figure 8-5. The first fiducial is located at the 0.0 location. The second and third fiducials are located in the X and Y directions from 0.0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all printed boards that contain surface mount as well as through-hole components since even through-hole assembly systems are beginning to utilize vision alignment systems.

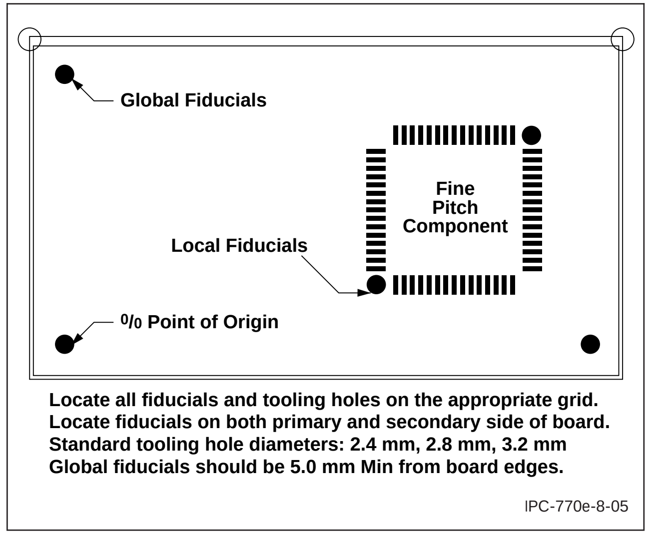


Figure 8-5 Fiducial Locations on a Printed Board

All fine pitch components should have two local fiducial systems designed into the component land pattern to ensure that enough fiducials are available every time the component is placed, removed and/or replaced on the board. All fiducials should have a solder resist opening large enough to keep the optical target absolutely free of solder resist. If

solder resist should get onto the optical target, some vision alignment systems may be rendered useless due to insufficient contrast at the target site.

If space is limited, a minimum of one local fiducial mark may be used to correct translational offsets (x and y position). The single fiducial should be located inside the perimeter of the land pattern with a preference for the center.

8.4.3 Size and Shape of Fiducial The optimum fiducial mark is a solid filled circle. The minimum diameter of the fiducial mark is generally 1.0 mm. The maximum diameter of the mark is 3.0 mm. Fiducial marks should not vary more than 25 µm in size on the same PB.

A clear area devoid of any other circuit features or markings should exist around the fiducial mark. The minimum size of the clear area should be equal to twice the radius of the mark. A preferred clearance around the mark is equal to the mark diameter (see Figure 8-6).

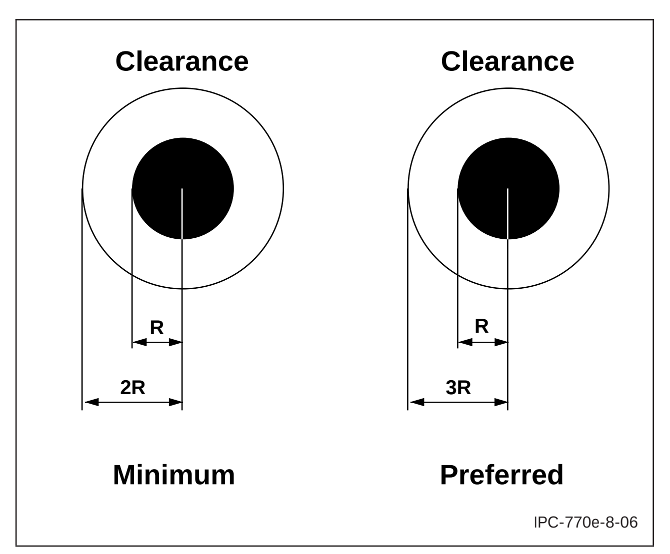


Figure 8-6 Fiducial Clearance Requirements

8.4.3.1 Material The fiducial mark may be bare copper protected by organic coating or metal plating. If solder resist is used, it should not cover the fiducial mark or the clearance area. It should be noted that oxidation of a fiducial mark's surface may degrade its readability.

8.4.3.2 Flatness The flatness of the surface of the fiducial mark should be within 15 µm.

8.4.3.3 Edge Clearance The fiducial mark should be located no closer to the PB edge than the sum of 5.0 mm and the minimum fiducial mark clearance required.

8.4.3.4 Contrast Best performance is achieved when a consistent high contrast is present between the fiducial mark and the PB base material.

The background for all fiducial marks must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must retain uniform background. If copper is clear under one fiducial, all must be clear.

8.5 Conductors

8.5.1 Conductor Width and Spacing Increased component density on SMT designs has mandated the use of thinner copper, narrower conductor width and spacing. Higher component density may increase PB layer counts requiring the use of more vias to make the necessary connections between layers.

8.5.1.1 Surface Layer Conductors As component count goes up and conductor width decreases, care must be taken to avoid conductor-to-pad or conductor-to-vias ratios of less that 2:1. Wide conductors-to-land areas can draw solder away from the land resulting in insufficient solder at the joint. If the conductor goes to a via connected to an inner layer, power or ground plane, heat may be drawn away resulting in a cold solder joint (see Figure 8-7).

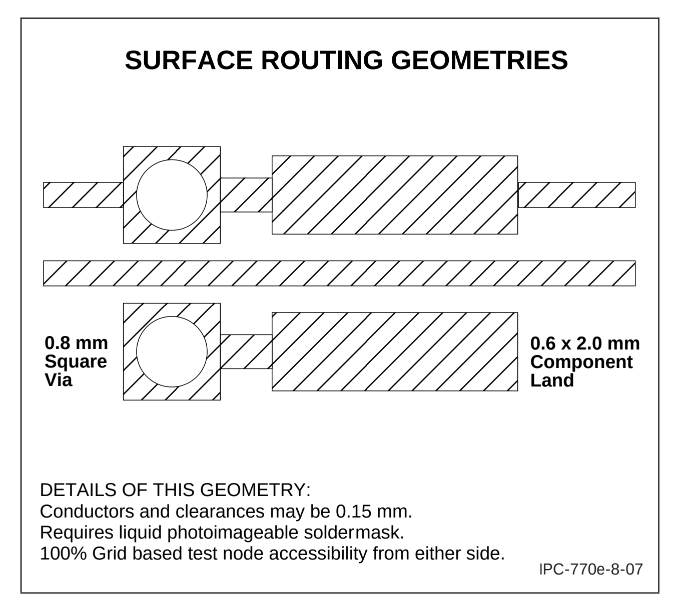


Figure 8-7 Surface Mounting Geometries

8.5.1.2 Inner Layer Conductors The use of wider conductors and spacing often drives layer counts up because there is less routing channel available between vias. It is for this reason that there is an increased usage of narrower conductors on internal layers. Since conductor width control is much more difficult to maintain on outer layers of the PB, it is better to keep the narrower geometries on the inner layers of a multilayer printed board.

8.6 Via Guidelines

8.6.1 Drilled Via Holes The size of the via holes should be selected on the basis of the printed board thickness versus the hole diameter or aspect ratio limits as defined by

the printed board fabricator. In addition, specific via lands and holes can be accessed for automatic in-circuit test (ICT). Figure 8-8 shows the land-pattern-to-via relationships.

Note: When attempting to reduce board thickness, the risk of unwanted bow and twist before and/or after soldering should be considered (see IEC 61188-1-1).

8.6.2 Vias and Land Pattern Separation Via lands must be located away from the component lands to prevent solder migration during reflow soldering. These migrations cause insufficient solder fillets on components. The solder migration can be restricted by providing a narrow conductor between the land area and the via or prevented by using the solder resist over bare copper circuitry. The relationship for mounting land and via locations should consider the conductor routing requirements. Figure 8-9 provides several examples of via positioning concepts.

Specifying solder resist tented or filled vias prevent solder migration on assemblies manufactured with a solder reflow process. Filled or tented vias also take care of potential flux entrapment problems under components and are highly desirable for attaining good vacuum seal during in-circuit bed-of-nails testing. Tenting is typically done with a dry film type of solder resist, or if via holes are very small, may be tented using liquid maskant.

8.6.3 Vias Under Components If the assembly is to be wave soldered, via holes underneath zero clearance components on the primary side should be avoided on boards unless vias are tented with solder resist. During wave soldering of the assembly, flux may potentially become trapped under zero clearance devices. Untented via holes may be located underneath zero clearance surface mount packages in reflow soldered surface mount assemblies that are not wave soldered.

8.7 Standard Fabrication Allowances Manufacturing tolerances or standard fabrication allowances (SFA) exist in all PB fabrication shops. Virtually every registration or alignment operation that is performed has some potential for error. This misregistration can affect art mounting and automatic placement. The tolerance varies according to the printed board maximum diagonal dimension and must be included in the land size calculations. The fabricator should be consulted prior to beginning a design to determine their SFA. With this SFA value, the designer can proceed accordingly, preventing tolerances from stacking up and creating yield and/or production problems.

8.7.1 Manufacturing Characteristics Figure 8-10 shows the various characteristics of conductor geometry after etching. End-product drawings and specifications should specify only the minimum for conductor spacing; however,

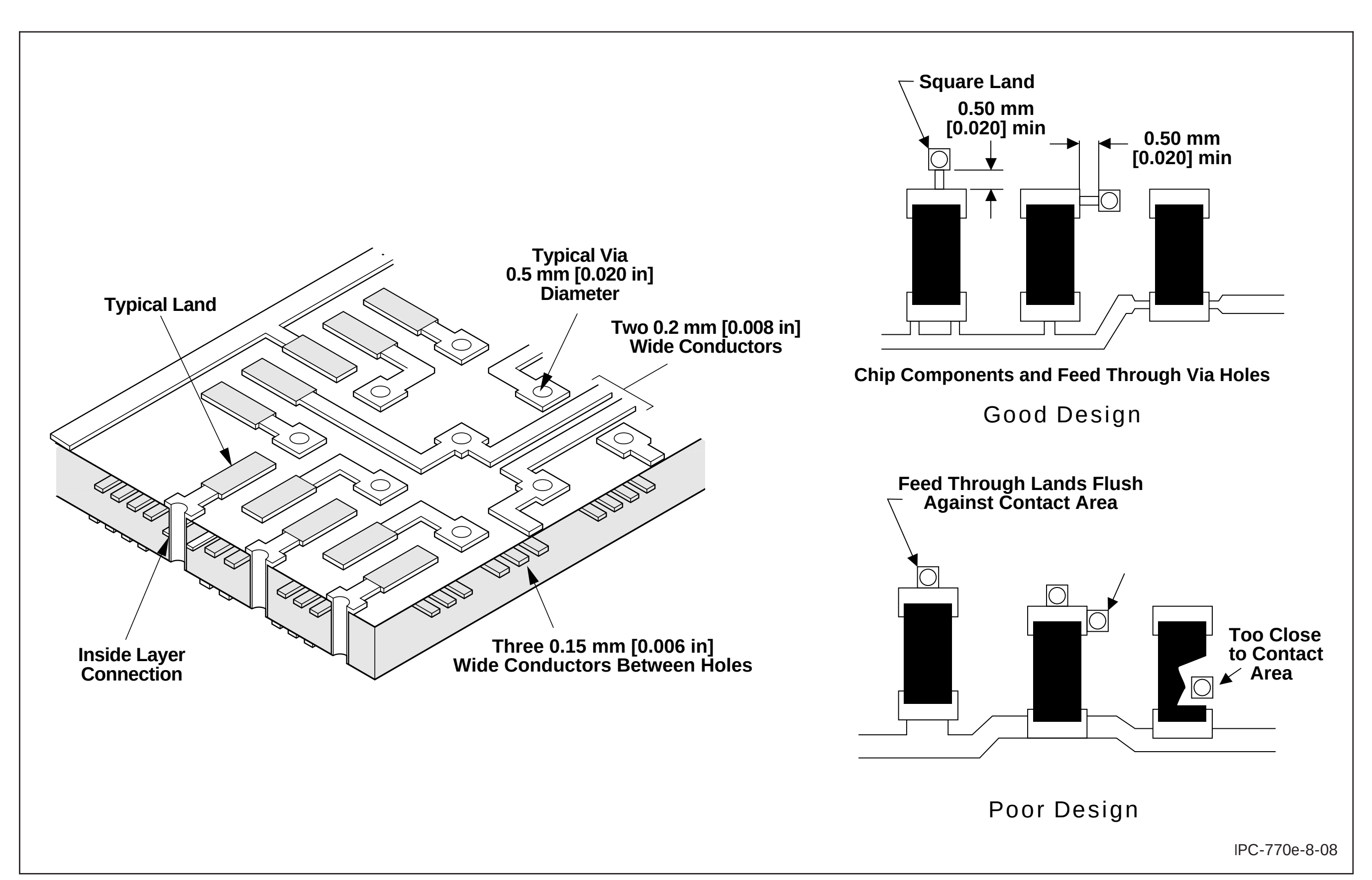


Figure 8-8 Land Pattern-to-Via Relationship

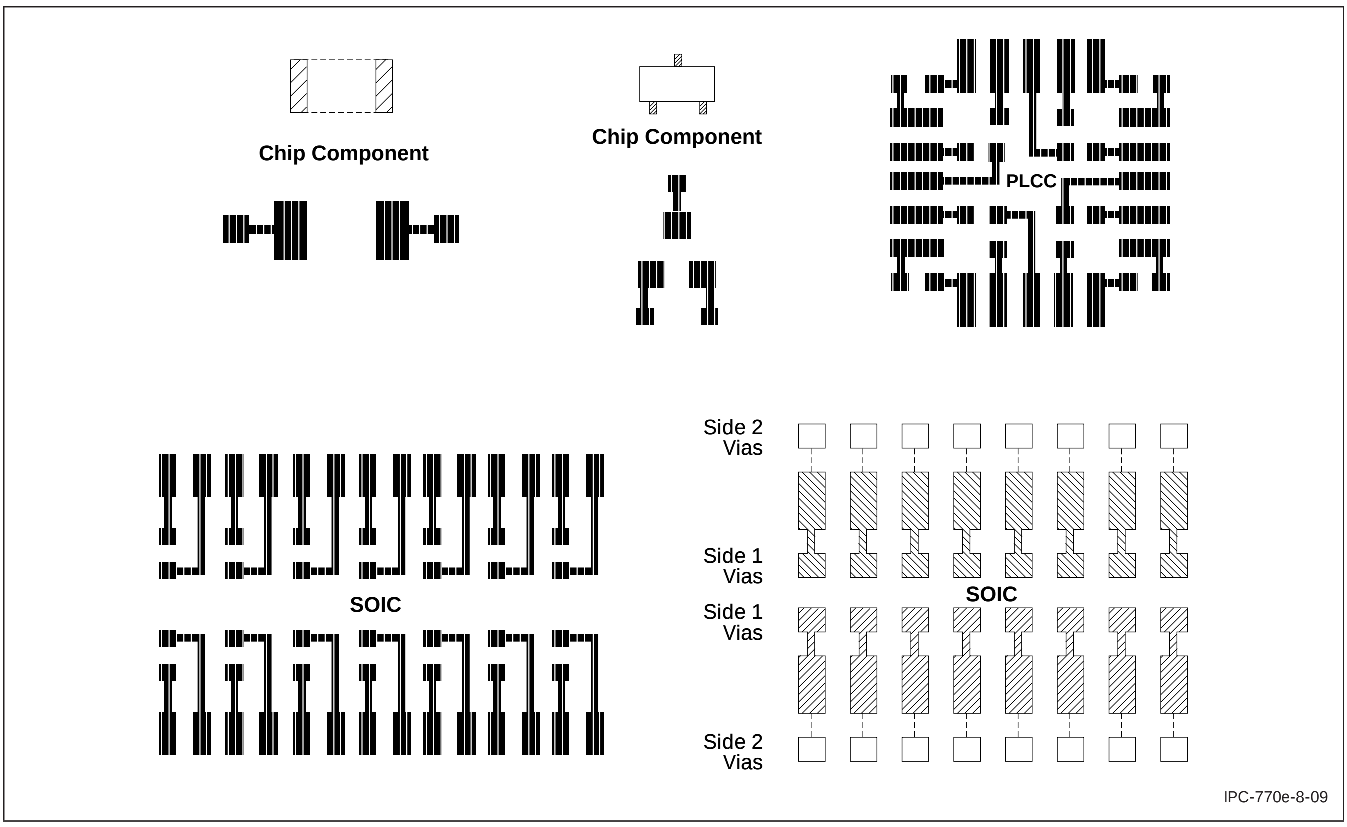


Figure 8-9 Examples of Via Positioning Concepts

conductor widths should be defined according to minimum values, where land patterns should be defined as to their maximum material conditions (MMC). Clear target values for conductors and land patterns help the manufacturer achieve the desired condition.

8.7.2 Conductor Width and Spacing Tolerances Table 8-1 represents process tolerances that can be expected with normal processing; specific process tolerances should be discussed with the board manufacturer. The tolerances are based on copper thickness up to and including 36 µm. For additional copper thickness, a further width variation can be expected (see Figure 8-10).

8.7.3 Conductive Pattern Feature Location Tolerance Table 8-2 is for the tolerance to be applied to the nominal dimension chosen for the location of the lands, connector contacts and conductors in relation to the datum reference. These tolerances include master pattern accuracy, material movement, layer registration and fixturing.

8.8 Board Size and Panelization In order to fully utilize the automation technology associated with surface mount components, a designer should consider how a printed board or P&I structure is fabricated, assembled and tested. Each of these processes, because of the particular equipment used, requires fixturing that affects or dictates certain facets of the board layout. Tooling holes, panel sizes, component orientation and clearance areas (both component and conductor) on the primary and secondary sides of the board are all equipment and process dependent.

To produce a cost-effective layout through optimum base material utilization, a designer should consult with the board manufacturer to determine optimum panel size. The board should be designed to utilize the manufacturer's suggested usable area. Smaller boards can be ganged or nested on this same panel size to simplify fixturing and reduce excessive handling during assembly. Most manufacturers suggest various methods of retaining assemblies in panels. A method should be chosen taking the assembly and test processes into consideration.

8.8.1 Panel Format Components can be mounted on individual boards or on boards that are organized in a panel form. Boards or panels that are moved by automatic handling equipment or pass through automated operations (parts placement, soldering, cleaning, etc.) must have specific areas kept free of parts or active circuitry. Typically, a clear ''keep out area'' of 3.0 mm to 5.0 mm wide should be allowed along the sides for the clearance. The required ''keep out area'' clearance width is dependent upon the design of the board handling and fixturing equipment. These dimensions should be obtained from the process equipment manufacturer before board or panel design (see Figures 8-11 and 8-12).

Special tooling and fixturing holes are generally located within the edge clearance areas. The clearance areas are

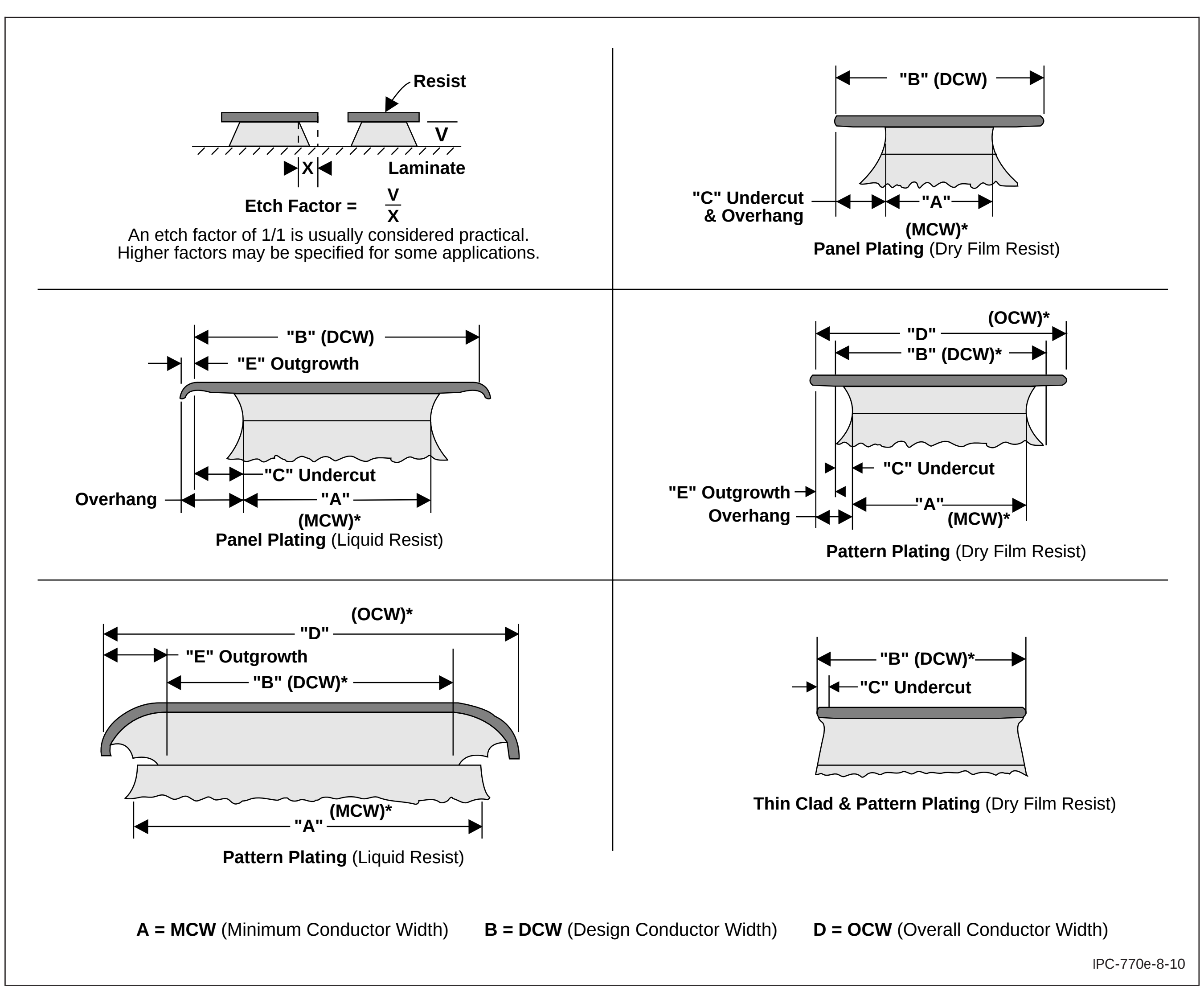


Figure 8-10 Conductor Description

Table 8-1 Typical Conductor Width Tolerances

Feature	Level 1	Level 2	Level 3
Without plating	+0.5 -0.10 [+0.002] [-0.004]	+0.03 -0.05 [+0.001] [-0.002]	+0.02 -0.04 [+0.0008] [-0.0016]
With plating	0.10 -0.10 [+0.004] [-0.004]	0.08 -0,08 [+0.003] [-0.003]	0.05 -0.05 [+0.002] [-0.002]

Table 8-2 Recommended Feature Location Accuracy

Greatest Board/ X/Y Dimension	Level A	Level B	Level C
Up to 300 mm [12.0]	0.30 mm [0.012]	0.20 mm [0.008]	0.10 mm [0.004]
Up to 450 mm [18.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]
Up to 600 mm [24.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]

needed to avoid interference with board handling fixtures, guidance rails and alignment tools. For accurate fixturing, two or more nonplated holes are located in the corners of the board to provide accurate mechanical registration on board transfer equipment. Board handling holes (typically 3.2 mm) may also be located in the clearance areas. These holes may be used by automated board handling equipment or for test fixture alignment. Specific panel size should be obtained from the equipment manufacturer or process engineer.

8.8.2 Panel Construction Panel construction may include several boards arranged in a matrix or consist of one board requiring additional material retained for efficient assembly processing. The large board or several smaller boards are retained in the panels and separated after all assembly processes are completed. Excising or separating the individual boards from the panel must be planned as well. Several methods are used to retain circuits in a panel, including V-groove scoring and routed slot with breakaway tabs.

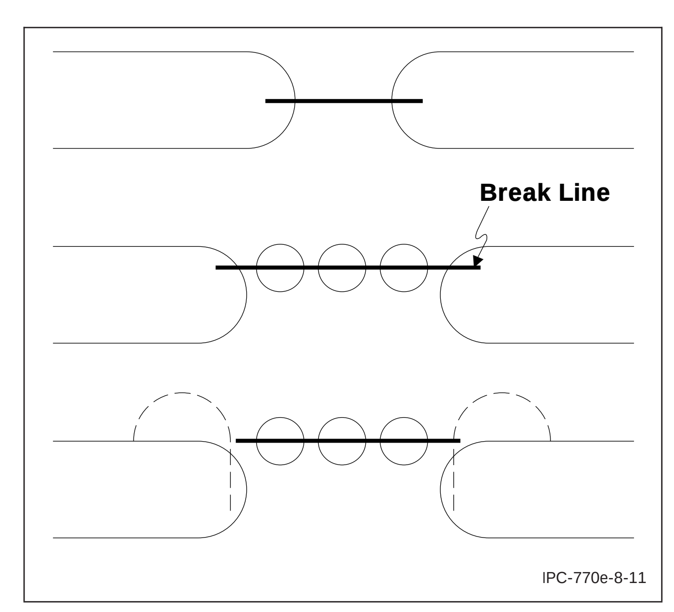


Figure 8-11 Routed Slots

V-groove scoring is generally provided on both surfaces of the board and only in a straight line. A small cross-section of board material is retained at the break line. An allowance for the scoring angle must be made as well. Conductors that are located too close to the score groove is exposed or damaged, and rough edges must be sanded lightly to remove burrs and rough fabric particles.

The routed slot and tab pattern is widely used for panel construction and breakaway tab extensions. Routing is more precise than scoring, and edge surfaces are smooth, but the breakaway ''tab'' points requires consideration. Tabs can be cut and ground flush with the board edge or predrilled in a pattern. The drilled pattern furnishes a low stress break point on the ''tab.'' If the hole pattern is recessed within the board edge, secondary sanding or grinding can be bypassed (see Figures 8-13 and 8-14).

Figure 8-12 Typical Copper Glass Laminate Panel

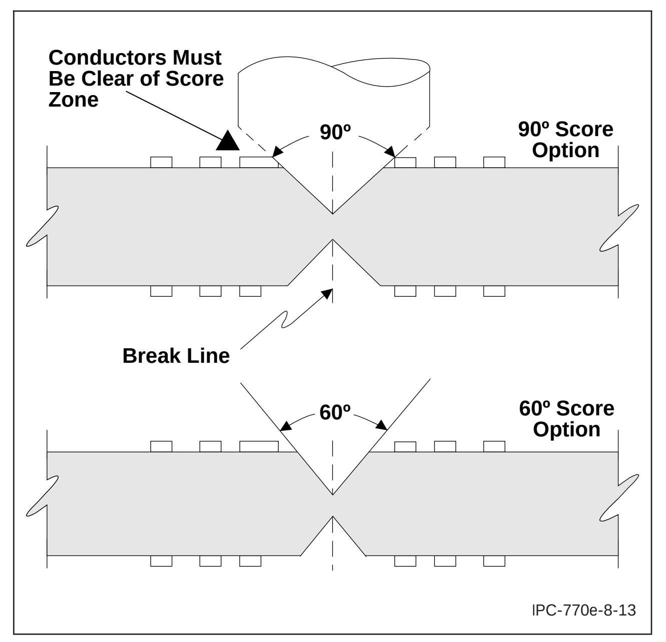


Figure 8-13 Conductor Clearance for V-Groove Scoring

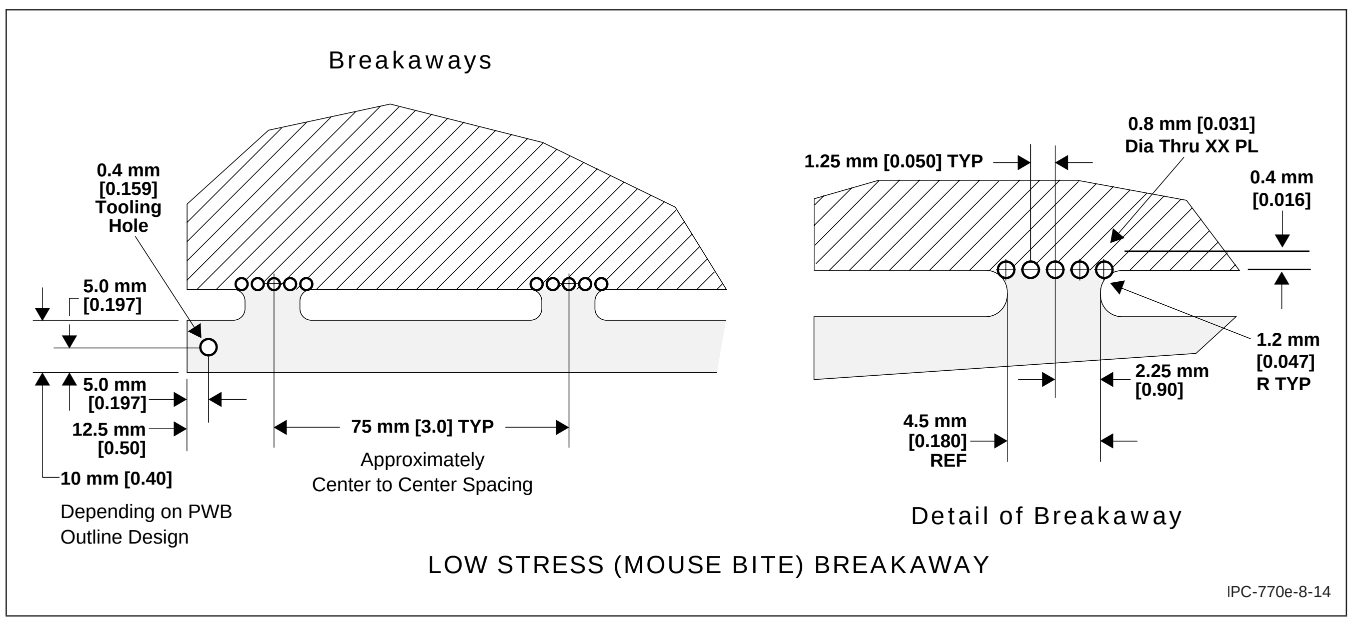


Figure 8-14 Breakaway (Routed Pattern) with Routed Slots

9 COMPONENT CHARACTERISTICS THROUGH-HOLE

All components used in a through-hole configuration have metal leads as the interface to the electronic elements of the component. The lead configuration may be round (pins), flat (ribbon) or V-shaped. Care needs to be exercised to assure leads are prepared and insertion controlled such that insulation on component leads does not extend into the hole. This condition can have adverse impacts on the resultant solder joint. This condition is often a problem with two-leaded disk type components not retained firmly in the hole. Such components tend to tilt before soldering introducing insulation in one hole and less than adequate protrusion in the other.

9.1 Axial-Leaded Discrete Components Axial-leaded components with two leads are perhaps the most common through-hole electrical components used in printed wiring assemblies. The component body is usually cylindrical in shape with two leads exiting from opposite ends of the component along its longitudinal axis. The lead is usually round in cross section. Component identification as well as polarity, when necessary, are generally marked on the body of the component. Many resistors, capacitors and diodes are supplied in this configuration (see Figure 9-1).

9.1.1 Packaging Axial Leaded Discrete Component Automatic processing technology and equipment handle

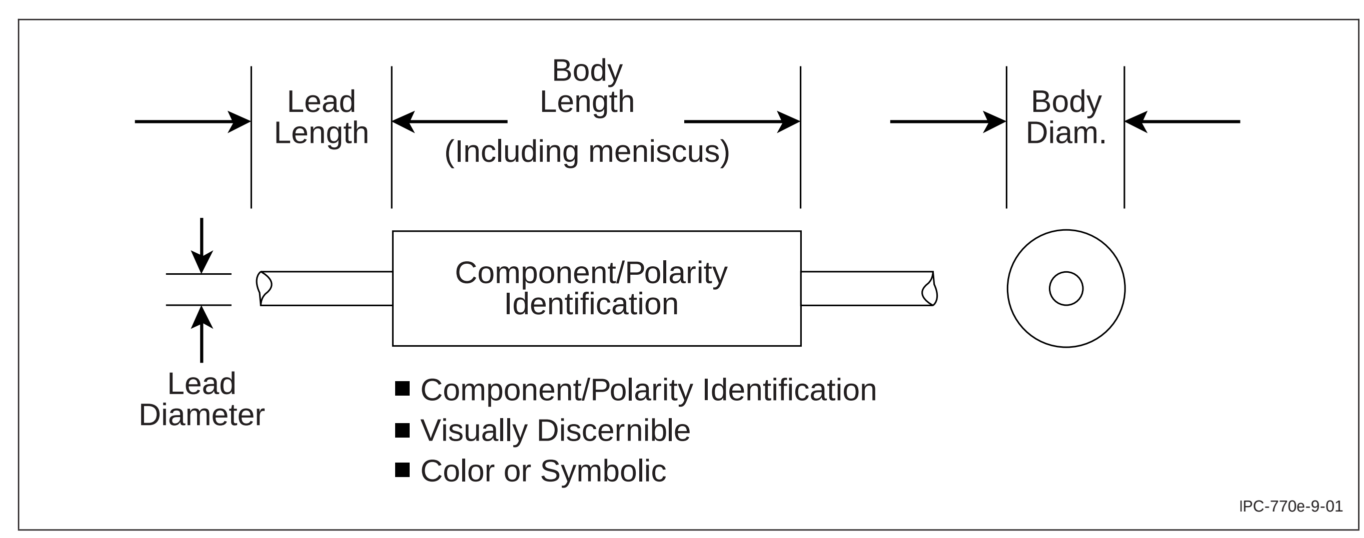


Figure 9-1 Axial-Leaded Component

this type of component very effectively when the components are provided in tape reels (see Figure 9-2).

In addition, axial-leaded components (two leads) can also come in polarized component body styles (see Figure 9-3). Size and material of component bodies and leads range and vary widely, based on device characteristics, electronic rating, and component package style techniques.

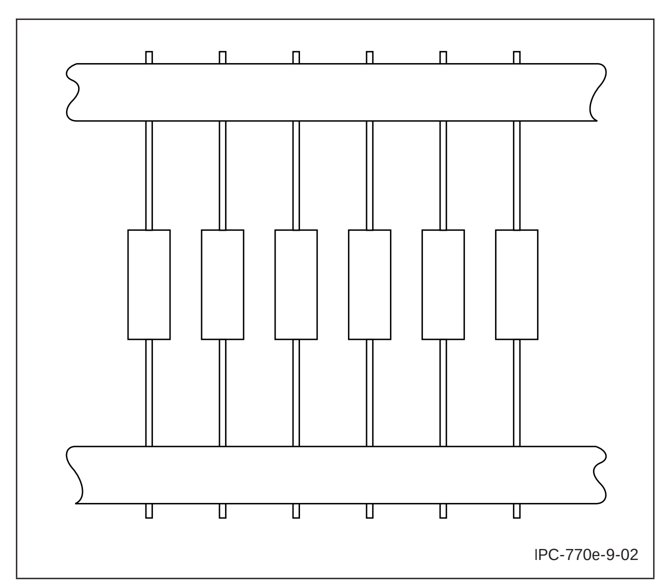


Figure 9-2 Taped Axial-Leaded Components

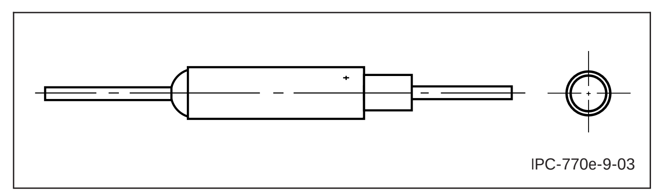


Figure 9-3 Polarized Axial Lead Component (Typical Polarity Markings)

9.2 Radial-Leaded Discrete Components Radial-leaded components come in a variety of shapes: cylindrical, square, rectangular, wafer and kidney. Leads exit from a common side of the component. The lead is either ribbon or cylindrical. Selected devices can be automatically inserted during assembly and also can be modified with coined leads for surface mounting.

9.2.1 Part Type Description Typical types of radial-lead components are electrolytic, plastic, dipped, molded and encapsulated capacitors and transistors (see Figures 9-4 through 9-7).

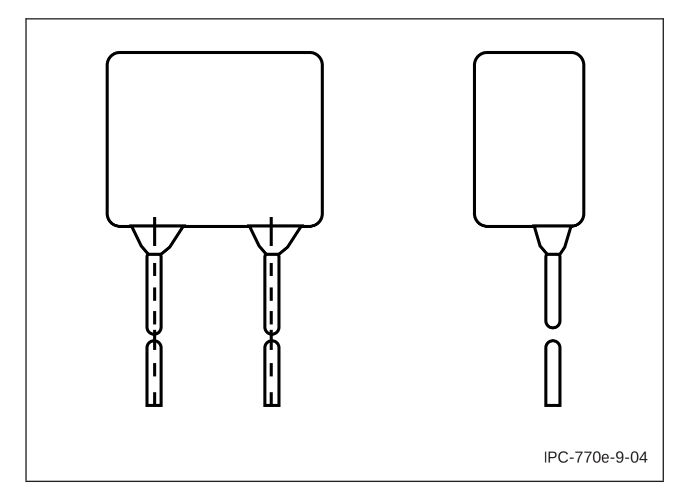


Figure 9-4 Rectangular Radial Lead Capacitors

9.2.2 Packaging Radial Leaded Discrete Components

9.2.2.1 Hermetically-Sealed Components Hermetically-sealed components such as electrolytic capacitors need to be handled with caution to prevent damage to seals. Bi-metallic welds should not be stressed.

9.2.2.2 Plastic Package Components The integrity of the interfacial adhesion between the plastic dip coating and encapsulant to packaging or leads needs to be maintained during handling.

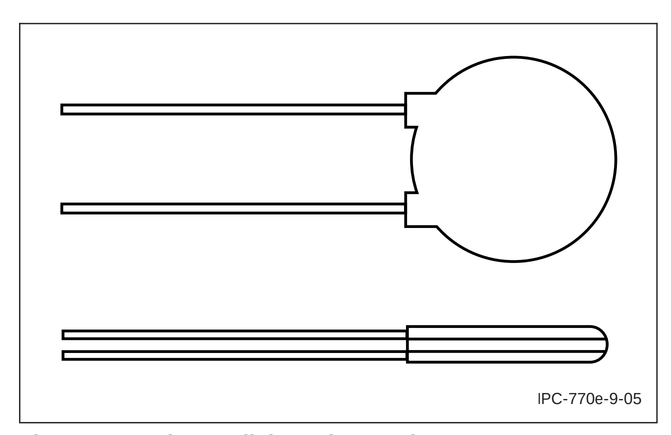


Figure 9-5 Disc Radial Lead Capacitors

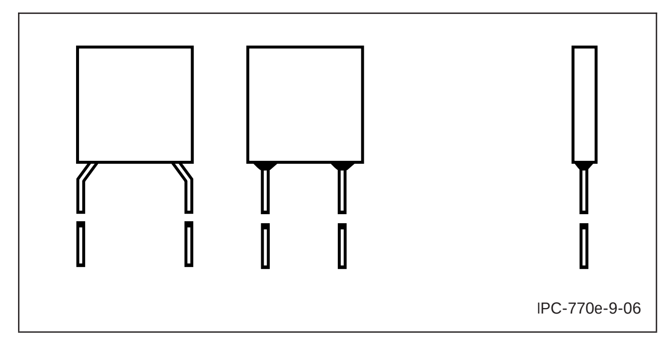


Figure 9-6 Cast Radial Lead Capacitor

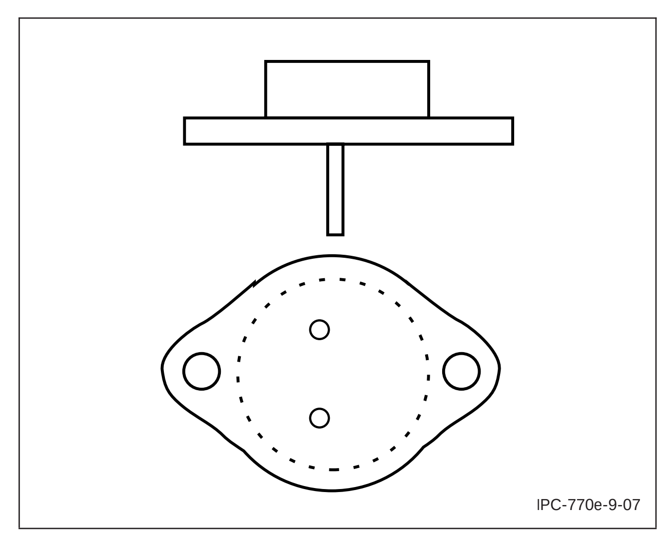


Figure 9-7 Radial-Leaded TO-3 Transistor Can

9.3 Multiple-Radial-Lead Components The packaging technology is well established for transistors in metal TO (transistor outline) cans. This configuration was used for early multiple lead components and is still popular today.

Multiple-lead component cans are also available in many sizes and shapes. The following general considerations should be taken into account when designing printed board assemblies with multiple-lead components:

- Land size, lead forming and lead clinching.
- The physical dimensions of the multiple lead component.
- Automatic, semiautomatic, and manual component insertion tolerances and restraints.
- Component dimensions and tolerances.
- Mechanical securing such as clips, clamps, brackets, sockets, etc.

9.3.1 Transistor Outline (TO) Cans This type of component consists of a hermetically sealed can with up to twelve round leads exiting from the bottom of the device (usually in a circular pattern). Dimensions of standard and registered TO devices are included in JEDEC 95-83.

Available tooling, hermetic sealing and a rugged construction made the can with 10 or 12 leads a natural first integrated circuit (IC) package. It requires special punching dies; drilling templates or off-grid numerically controlled (NC) drill programming for the 5.84 mm diameter pin circle.

9.3.2 Multiple-Lead Variable Resistors Figure 9-8 is an illustration of one type of multiple leaded variable resistors.

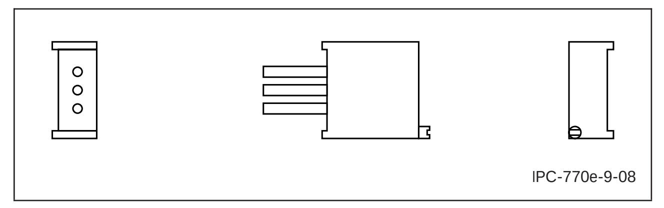


Figure 9-8 Multiple-Lead Variable Resistor

9.4 Inline Packages

9.4.1 Dual-Inline Packages The dual-inline, multiple-lead component (DIP) has its lead pointing downward ready for insertion into holes in a printed board.

The dual-inline package can be inserted easily, either automatically or manually. Sockets are available for mounting and testing purposes. Automatic insertion is very feasible using this package configuration.

A DIP is made of metal, ceramic, glass, plastic, or combinations of these materials. Leads, body, and glass sealing are designed to make this a rugged package. Lead configuration (shoulder) provides a standoff feature. Leads clinched into a 10 ± 5° ‘‘V’’ formation provide retention of the component (see Figure 9-9).

9.4.2 Single-Inline Packages The single inline packages (SIP) components are similar to the dual-inline (DIP) components. The leads exit the component body ‘‘inline’’ 2.54 mm apart, center to center pitch. However, the single-inline packages have in a single row pattern rather than the dual row (square) pattern of the DIP (see Figure 9-10).

Single-inline packages (SIP) component configuration is usually associated with resistor networks and can therefore

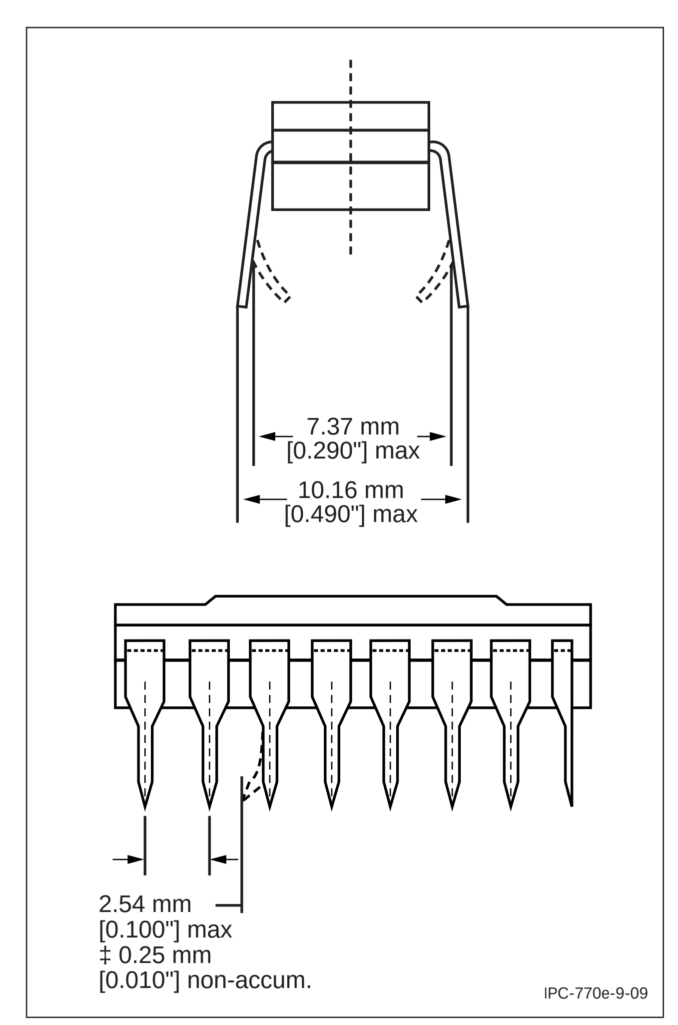


Figure 9-9 16-Lead Dip

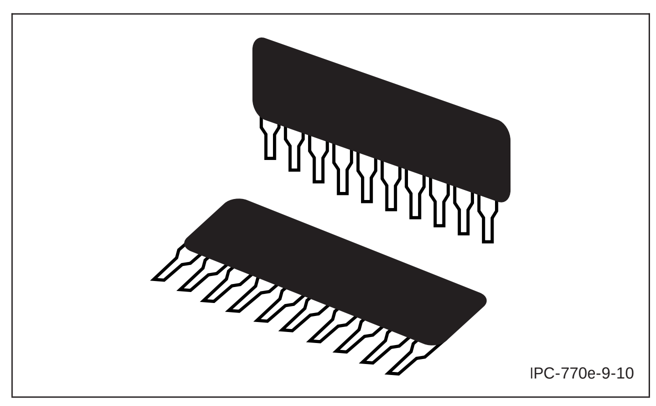


Figure 9-10 Single Inline Packages Component

reduce handling, inventory, and assembly requirements by the use of a single component, versus a number of discrete components. Advantageous uses of the SIP type component are applications where printed board real estate is limited.

9.5 Ribbon-Lead Components Flatpacks and quad packs are similar to small outline package (SO) devices, but also have many important differences. The vendors normally supply these devices with the leads extending straight out from the body on two opposite sides, or from all four sides. Although this requires the user to form the leads, this permits either surface-mounting or through-hole mounting techniques. SO device leads are preformed by the vendor for surface mounting only.

These devices are available in both hermetically sealed and molded plastic styles. Hermetically sealed devices are packaged in metal, ceramic, glass, or combinations of these materials. SO devices are normally available only in molded plastic cases.

Multiple-ribbon-lead components are highly suitable for high density printed board applications due to their close lead spacing, 1.25 mm, and small body sizes. The wide variety of flatpack configurations permits a wide variety of mounting methods.

The basic flatpack mounting technique can be categorized as being either the through-hole mounting or surface mounting. This section only includes the through-hole mounting (see Section 2 for Surface Mounting Guidelines). Through hole mounting can be divided into the following categories:

- Unclinched lead.
- Clinched with circumscribing full land.
- Clinched with offset land.

A number of discrete devices (transistors and diodes) are also available as ribbon leaded devices. Most of these have been designed specifically for high frequency, stripline mounting.

9.5.1 Flatpack One of the smallest of the presently existing multiple lead component types is the flatpack. The body of these components can be as small as 3.2 mm wide, 6.4 mm long and 0.8 mm thick. The component leads are normally flat ribbons 0.5 x 0.25 mm or smaller, and are located on 1.27 mm centers. Flatpacks are presently available with up to 50 leads. Various approaches are used to facilitate the securing of these to carriers:

- Form leads to fit a staggered hole-land pattern, using pot or wave soldering.
- Weld or solder leads to lands or tabs.
- Simultaneously solder-coat all leads and then reflow-soldered. (For leads with stress relief bends, since this protects the glass seal welds or solder to lands or tabs that are 0.8 mm wide x 1.9 mm long.)

Flatpacks must be insulated when placed over conductive traces. Unless the user has control over the particular package material, it may be appropriate to provide insulation between the bottom of the flatpack and any conductive traces, regardless of the case material being used.

Users of flatpacks have had problems as a result of nonstandard shipping containers. Another flatpack problem is that the automated assembly cost is very high compared to

other packages, owing to the fragile leads and the special care required in assembly.

Flatpack devices are usually of the outline depicted in Figure 9-11. Dimensions of standard flat pack devices are listed in MIL-M-38510 and in JEDEC publication 95-83.

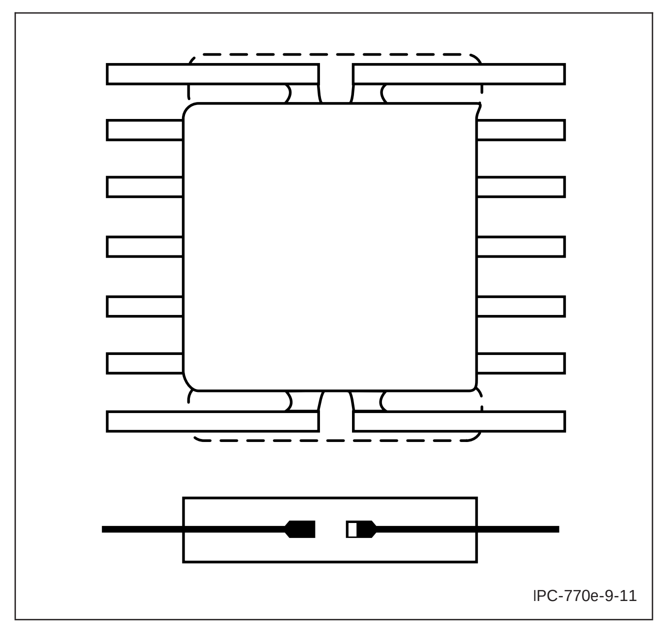


Figure 9-11 Flatpack Outline Drawing

9.5.1.1 Flat Pack Device Type One of the smallest multiple lead components is the flat pack. The body of these components can be as small as 3.18 mm wide, 6.35 mm long, and 0.79 mm thick. The component leads are normally flat ribbons 0.5 x 0.25 mm or smaller, and are located on 1.27 mm centers.

Through hole mounting of flat packs is accomplished by forming the leads to fit an appropriate hole-land pattern. Attachment is then accomplished using either pot or wave soldering.

9.5.1.2 Discrete Device Type Ribbon leaded discrete devices are also very small leaded discrete devices. The case is normally no larger than necessary to provide mechanical support for the leads. These devices were originally developed for use on stripline boards, where the part body is recessed into the board so that the part leads are aligned with the stripline circuit traces.

The special characteristics of these devices (small lead inductance, low capacitance between leads, and small physical size) have also made these devices useful in non-stripline applications. Figure 9-12 shows a typical ribbon leaded device with flat leads. JEDEC publication 95 lists the dimensions of ribbon leaded discrete devices.

9.6 Pin Grid Array Components The advent of very large scale integration (VLSI) and very-high-speed integrated circuit (VHSIC) has brought a need for very high

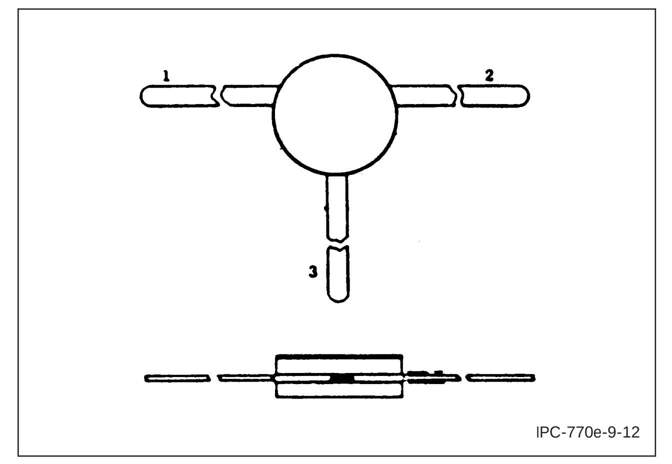


Figure 9-12 Typical Ribbon Leaded Discrete Device Outline Drawing (Flat Leads)

pin count packages with lead symmetry and methods to reliably assemble them onto circuit boards.

Grid arrays are pinned or leadless carriers with I/O contacts that populate one surface of the package on a grid 2.54 mm or smaller. The use of a solid grid necessitates placing the die cavity on the side opposite the I/O contacts. A double or multiple concentric row grid permits having die cavity and I/O contacts on the same side with an optional heat sink on the opposite side.

The pin grid array package is designed for high pin out ICs for through-hole mounting because of its space efficiency and compatibility with existing DIP facilities.

The main advantage of the pin grid array is to avoid the I/O limitations of peripherally terminated packages such as LCC, at the same time providing terminal separations of 2.54 mm centerlines. As such it can be readily installed into a conventional printed board and also wave soldered. The disadvantages are as follows:

• Inspection of solder joints
• Impedance limitations
• Removal and replacement

A typical pin grid array is a square, multilayer (usually ceramic) package having terminals on 2.54 x 2.54 mm centers. These packages are available in either cavity up or cavity down versions.

A cavity up configuration mounts the die opposite the pins, thereby allowing a full grid of pins and the highest I/O density. A cavity down configuration has the die on the same side as the pins and is generally used with high power circuits in air-cooled applications to allow a heat sink opposite the die. However, this version is not as space efficient.

Pin grid arrays have good electrical characteristics due to the short signal paths from I/O pin to die. Pin grid arrays overcome thermal expansion problems typically encountered at ceramic/printed board interfaces because the pins

are compliant. Conventional soldering techniques such as wave soldering can attach these packages to printed boards. The higher the I/O lead count, the lower the percentage of the total package area the die cavity occupies, e.g., the 96-lead, 1.02 mm center chip carrier is over one-inch square. For optimum packaging density, this percentage should be as high as possible. Therefore, 0.635 and 0.5 mm chip carriers and grid arrays are used (see Figure 9-13).

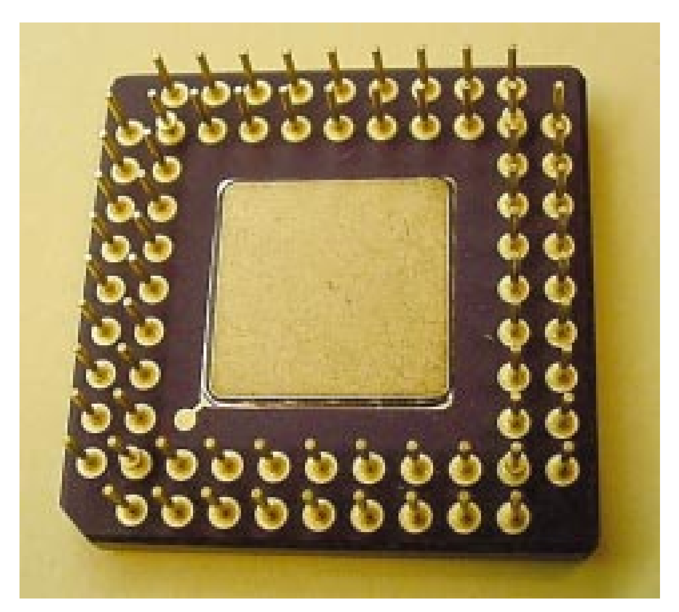


Figure 9-13 Pin Grid Array

Figure 9-14 shows the I/O density achievable with the various packages. For lead count requirements in excess of 100, a 2.5 mm centerline solid grid provides greater I/O density than either 1.27 mm or 1.02 mm centerline chip carriers.

The 0.635 mm centerline chip carrier is clearly more I/O efficient than is a 2.54 mm grid array. However, a double-row 1.27 mm solid grid provides the greatest I/O density. With pins brazed on 2.54 mm centers, pin grid arrays are a logical carrier for high lead counts intended for through-hole (not surface mount) board assembly compatible with DIPs. This should extend the useful life of present day technology for some high lead count applications.

9.7 Through-Hole Mount Connectors Through-hole connectors are designed to mount to the printed board with the leads extended through the board. The leads are then typically soldered in place to permanently mount the connector to the board. A variety of connectors, employing a compliant section in a pin, are available. The compliant section allows installation in a plated-through hole without the need for soldering. The interference fit between the compliant section of lead and plated-through hole achieves a reliable gas tight interconnection. Installation of this type requires the use of an arbor press with suitable tooling (see Figure 9-15).

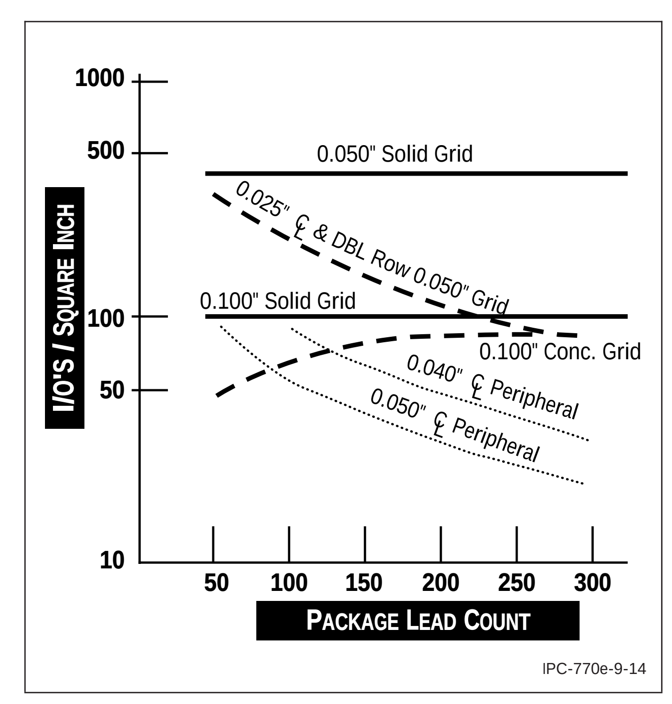


Figure 9-14 I/O Density Versus Lead Count (All Dimensions in Inches)

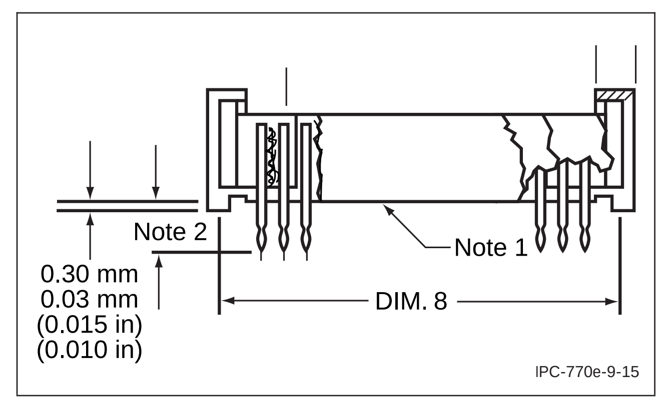


Figure 9-15 Connector with Press Fit Contacts

Connectors may be mounted to the printed board by soldering, welding, crimping, press fitting or other means. Leads may be extended through hole or contacted to circuit lands provided on the board. Holes may be plated through or simply drilled. The exact method depends on the connector design. Board size and weight are important factors in choosing connector-mounting hardware, and in deciding whether the board is mounted horizontally or vertically. It is common practice to mount the connector either to a mother board or to card racks or frames, then insert the component board into the connector using appropriate guiding and support mechanisms. In general, if the board is mounted horizontally, or if vibration is to be encountered, the board should be attached to the connector or supported by mechanical means other than contact.

Press fit headers require special tooling to apply the header to a board. Tooling can vary from simple hand fixtures to

elaborate presses depending on part size and connector design.

Connectors with low line densities can be installed manually. Higher concentrations require card ejectors, jacks, or guide pins. Zero insertion force connectors are available, which require an auxiliary force to make connections after the card is inserted into the connector.

Note: Many versatile connectors are available for the printed board designer to transfer signals or power to the boards. Careful attention to the uses and requirements of these devices will result in reliable interconnections.

Connectors with integral retention to the board are favored for manufacturing ease. Connectors that cannot be snapped or clinched in place prior to soldering require mechanical fastening. This is primarily for positioning and the connector must then be soldered to assure electrical integrity.

Examination of the leads is recommended. The assembler should look for grossly bent leads, poor plating and loose debris.

9.8 Through-Hole Sockets Sockets normally have preset leads and are usually supplied by vendors and are prepared for assembly into the board. Preparations should be focused into two areas:

- Selection of the component (and its options) for particular assembly.
- Assurance that the part is supplied as requested.

The best guarantee is a preproduction trial run of the assembly. Areas of concern are:

- ***Packaging and Handling –*** Inadequate or improper methods damage lead sets that forces line delays.
- ***Terminal Surface –*** These should be provided with tinned or gold plate. Uncoated terminals must be pretinned.
- ***Length of Terminals –*** The terminals should not protrude beyond the board more than 1.5 mm and should be discernible in solder joint.
- ***Seals –*** The assembly (solder, cleaning, etc.) dictates the degree to which the component must be closed. Standard precaution, however, requires use of a closed entry bottom terminal exit or a plate to achieve the same effect. Special tapes or pallet tools can seal the socket face when needed.
- ***Cleanliness –*** Wave solder assembly cleaning processes are normally adequate to assure part cleanliness. Periodic examination of preassembly components is a normal procedure.

For applications where speed and ease of installation and removal are major considerations, devices can be mounted in suitable sockets. Sockets can be used in through-hole (nonsurface mounting) applications (see Figure 9-16). However, since the terminals of the chip carrier are not on 2.54 mm centers, a contact similar to the one shown in Figure 9-17 is used to provide the desired transition. A polarizing boss can be provided on the connector to mate with a corresponding hole in the printed board structure.

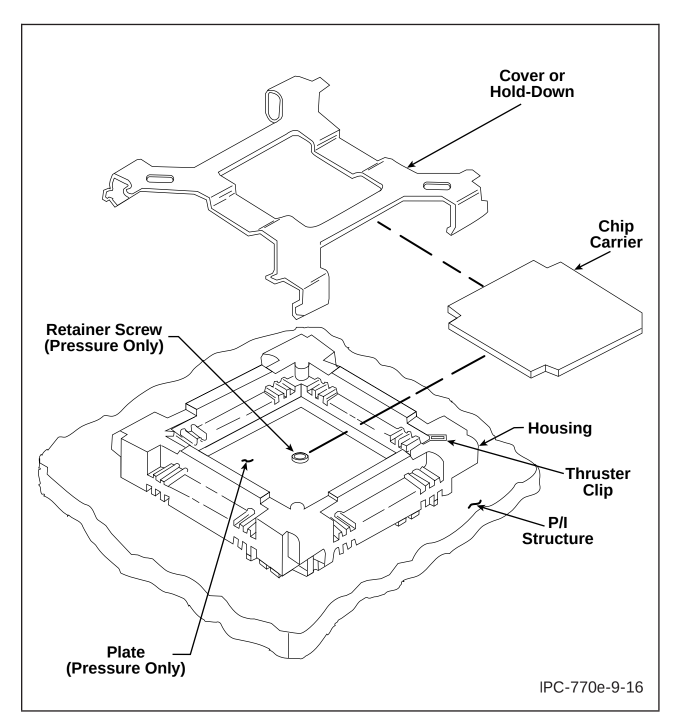


Figure 9-16 Surface Mount Clip Carrier Socket

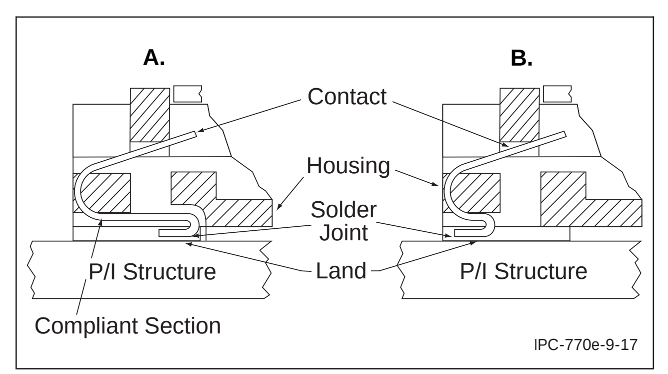


Figure 9-17 Section Through Socket Solder Contact

The low profile plastic leaded chip carrier socket serves as a transition device to enable users to take advantage of the benefits of four-sided IC packages without making changes in their current assembly procedures.

As previously mentioned, the chip carriers can have surface mount leads on 1.27 mm spacing. The chip carrier socket has flat spring input leads on 1.27 mm spacing to accommodate the package, and straight solder tail output leads on 2.54 mm spacing to meet the requirements for standard through-hole mounting.

Through-hole mounting is the dominant choice for pin grid array packages. Sockets for pin grid arrays are designed to match pin configurations.

There are three types of pin grid array sockets currently available:

- ***Standard Version –*** Allows the component to be pushed in.
- ***Low-Insertion Force –*** Employs a low force contact design.
- ***Zero-Insertion Force –*** Makes use of a mechanical assist to maintain contact pressure.

10 MOUNTING STRUCTURE REQUIREMENTS THROUGH-HOLE

10.1 Printed Board Characterization and Types Printed boards may be rigid, flex and rigid flex or combinations thereof.

10.1.1 Lead/Hole Ratio The lead-to-hole ratio must provide adequate clearance for good soldering conditions. If the clearance is too small or too large, adequate wicking of solder does not result. For rectangular leads, the dimension across the diagonal should be considered as being the lead diameter (see IPC-2222).

10.1.2 Unsupported Holes In determining the difference between the diameter of an unsupported hole and that of the lead to be placed in the hole, the hole should be from 0.25 mm to 0.5 mm larger than the lead diameter. Leads should be clinched when going through unsupported holes.

10.1.2.1 Diameter of Unsupported Holes When using the basic dimensioning system, holes are to be expressed in terms of maximum material condition (MMC) and least material condition (LMC) limits. The diameter of an unsupported component hole are to be such that the LMC of the lead subtracted from the MMC of the hole provides a clearance between a minimum of 0.15 mm and a maximum of 0.5 mm. The number of different hole sizes is to be kept to a minimum. When flat ribbon leads are mounted through unsupported holes, the difference between the nominal diagonal of the lead and the inside diameter of the unsupported hole should not exceed 0.5 mm and should not be less than 0.15 mm.

10.1.3 Supported Holes To determine the difference between the diameter of a supported hole and that of the lead (see IPC-2222).

10.1.3.1 Diameter of Plated-Through Holes The maximum and minimum plated-through hole diameters used to attach component leads or pins to the printed board should be evaluated in accordance with IPC-2222. Both minimum and maximum leads need to be taken into consideration in evaluating the finished plated-through hole requirements. If the lead is a ribbon lead, the minimum and maximum diagonal of a flat ribbon lead needs to be considered. IPC-2222 shows the limits of the plated-through hole.

These limits need to be optimized so that manufacturability is enhanced to provide the most liberal tolerances allowable (see IPC-2222).

10.1.4 Axial and Radial Lead Component Mounting Land patterns must consider minimum/maximum lead spacing requirements. Standard land spacing patterns should be established for the purpose of uniformity of assemblies and the practical use of assembly tools and equipment. Spacing(s) should be designed to accommodate automatic assembly and ‘‘bed-of-nails’’ testing equipment (usually in 2.5 mm increments, e.g., 7.5 mm, 10 mm, 12.5 mm, etc.).

Land patterns for unsupported holes should have larger solderable area than that for supported holes for a stronger joint after soldering. The optimum dimension is dependent on the device and its mounting characteristics. The most common geometry is the round land with a centered hole. Square lands with centered holes are sometimes used to indicate polarity for polarized components.

10.1.5 Multiple Radial Lead Component Land Patterns Land Patterns for multilead radial packages are a function of the dimensions and number of leads as they exit the body of the component to be mounted. Pattern configuration may vary depending upon the lead forming requirements.

In Figure 10-1, the leads of a TO-100 are formed to a standard 6.4 x 9.5 mm pattern, leaving space for two vias or plated holes available for internal plane connections or for conductor routing.

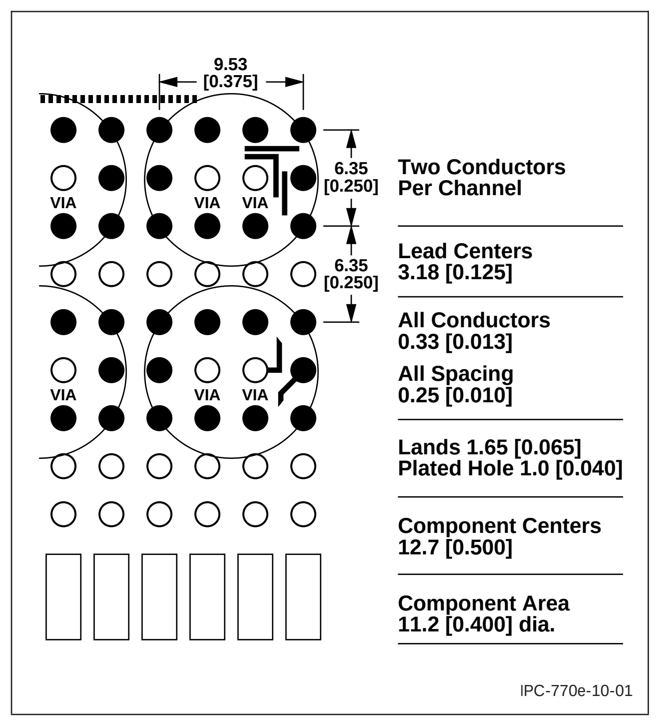


Figure 10-1 Typical TO-100 Can Layout

A typical printed board-mounting pattern for 10-lead multiple-lead cans with a 5.84 mm lead circle, such as TO-96, TO-97, and TO-100, is shown in Figure 10-2. The small lead circle dimensions require accurately located lands, of a small diameter, with minimum annular rings.

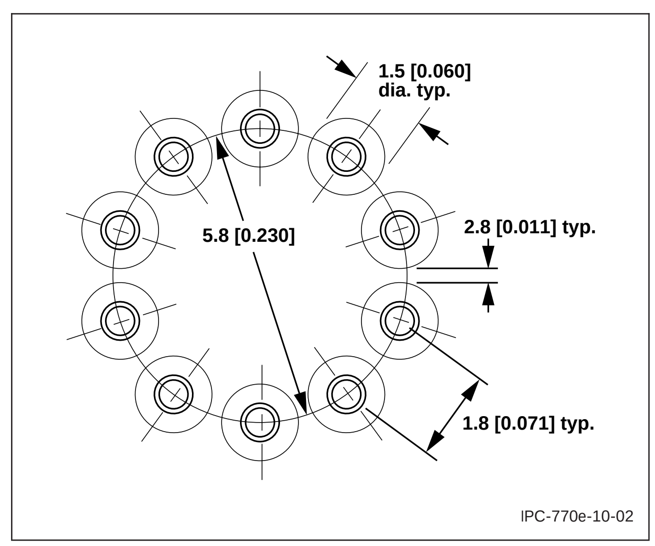


Figure 10-2 Typical Mounting Pattern for 10-Lead Cans with Clinched Leads

10.1.6 Dual-Inline Package (DIP) Land Patterns DIP layouts usually follow a rectangular grid pattern and reasonable densities are possible, such as that shown in Figure 10-3.

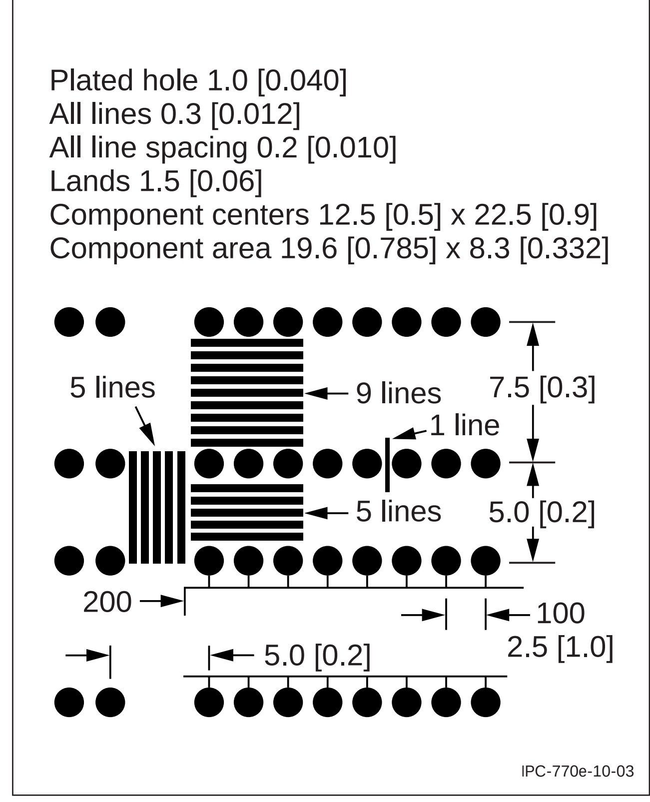
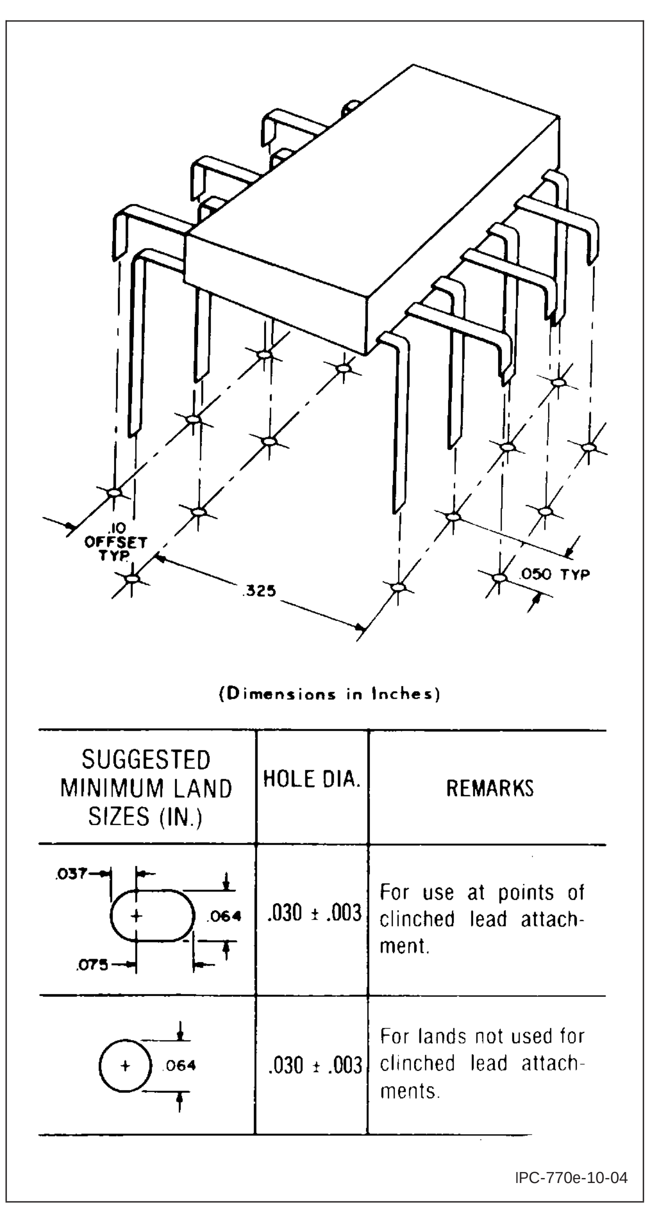


Figure 10-3 A Typical Dual-Inline Layout

10.1.7 Land Patterns for Ribbon Lead Component Typical land patterns for through-hole mounting are included in Figure 10-4. The inline-mounting pattern is much more restrictive regarding tolerances and position because of the limited space between the leads.



SUGGESTED MINIMUM LAND SIZES (IN.)	HOLE DIA.	REMARKS
.037, .064, .075	.030 ± .003	For use at points of clinched lead attachment.
.064	.030 ± .003	For lands not used for clinched lead attachments.

Figure 10-4 Staggered Hole Pattern Mounting (Flatpack Outline Drawing)

The staggered lead arrangement of Figure 10-4 permits hole sizes of 0.75 mm, which accommodates ‘‘F’’ outline devices under all combinations of hole diameter and lead size tolerances. The size and shapes of the solder-land terminations for flatpack integrated circuits depends on whether ‘‘inline’’ or ‘‘staggered’’ terminal configurations are used. The sizes and shapes of lands for TO type packaged circuits depends on the effective lead-circle diameter.

10.1.8 Land Patterns for Pin Grid Array Component When mounted directly to the printed board, land patterns

are developed according to the applicable class of the assembly. However, the preferred lead/hole ratio should allow for placement variables and good capillary action of solder flow.

10.1.9 Land Patterns for Through Hole Mount Connectors Connectors are available for a variety of land patterns, including inline and staggered. Commercially available pitches are 1.27 mm and greater.

10.1.10 Land Patterns for Through Hole Mounted Sockets The socket supplier usually offers the most appropriate board layout for the component. Automatic assembly normally demands additional clearance for greater positioning/placement allowance.

Sockets are somewhat unique to other board components in that they serve as a connector housing for their components. As such, they create more stress/strain on the fillet through the terminal, and therefore it is strongly recommended that:

- Surface land diameters be as large as allowable.
- The PTH diameter should be designed to allow maximum capillary action.

11 ASSEMBLY SEQUENCE THROUGH-HOLE

11.1 Process Steps Because of the multistep component mounting operation, the designer of intermixed assemblies must take into account all of the fabrication and assembly steps necessary to complete the electronic assembly. Concerns during the design cycle include:

- Component Types
- Assembly Process (Single and double-sided assembly, component securing)
- Joining Techniques (Single and double-sided joining techniques, required care for heat sensitive components, handling of unsealed components)
- Sequence of Events

11.1.1 Sequence The selection of a particular method for mounting and connecting components in equipment depends on the following: the type of component package involved; on the equipment available for mounting and interconnecting; on the connection method used (soldered, welded, crimped, etc.); on the size, shape, and weight of the equipment package; on the degree of reliability and maintainability (ease of replacement) required; and on cost considerations. Figure 11-1 shows a typical component mounting sequence.

Tests performed on clinched leads show that the pull and yield stresses produced by lead-clinching operations are far below the allowable limits for these leads.

11.1.2 Attachment Issues Component preparation is the processing step, which generally includes forming and cutting of component leads to facilitate subsequent component assembly and/or minimize component damage due to stress.

In any method which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the seal, and that forming be done with extreme care to avoid damage to lead plating. Bending, forming and clinching of component leads produce stresses in the leads and can cause stresses in the seals if precautions are not taken. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads such as those used in dual-inline or flat-packaged integrated circuits, less than the lead thickness. It is also extremely important that the lead exiting the body of the component is parallel to the axis of the component, and that the ends of the bent leads be perfectly straight and parallel to assure proper insertion through the holes in the printed board.

The most significant advantage of using the through-hole mounting method is its compatibility with conventional mass soldering techniques, such as dip and wave soldering. In addition, replacement of flatpacks mounted in this manner is readily accomplished by melting and removing the solder from each land individually or in multiples.

Parts and components should be mounted on the side of the printed board opposite the side that contacts the solder if the board is machine soldered. Except when mounted in cordwood modules or on unrepairable printed boards, parts and components should be spaced and located so that any part can be removed from the printed board without removing another part.

11.1.3 Assembly Process Methods The assembly process methods for attaching components to the printed circuit assembly typically uses solder as the medium to create the electromechanical connection of the solder joint.

The component preparation process may not cut the component leads to the desired length for all components and all applications. The reasons may vary, but they all relate to the methods of handling the product prior to the soldering operation. During assembly many of the leads are physically bent over to secure the component in place, while others are left straight, as they are not pushed up through the board during the soldering operation. After soldering, these long leads should be trimmed to prevent shorting to the adjacent products when used in their final application.

Many lead-trimming methods were previously used but the one that maintains its tenure is the solder-cut method. This method simply utilizes the soldering process to secure the components then the trimming is performed manually, semiautomatically or automatically.

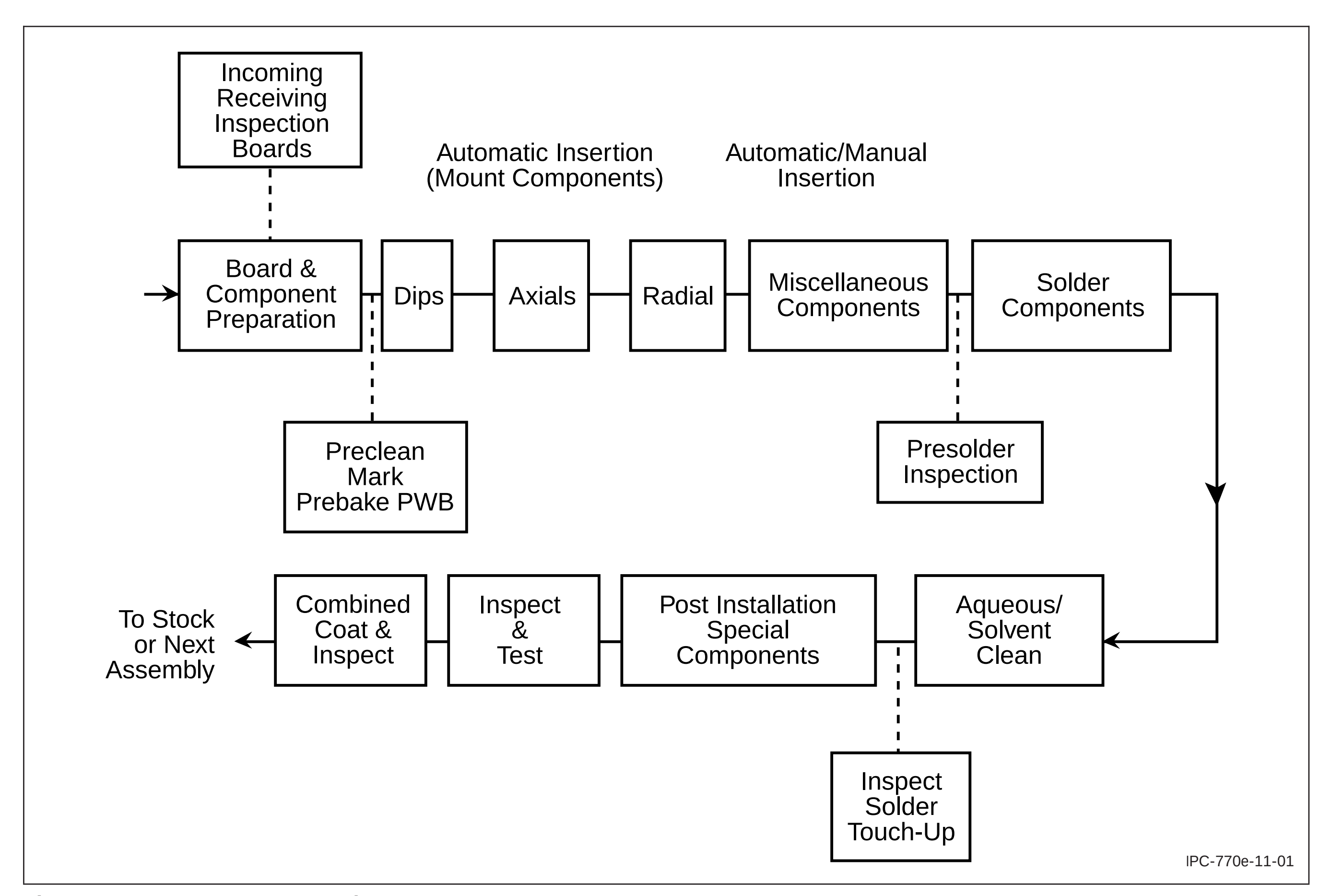


Figure 11-1 Component Mounting Sequence

Per J-STD-001, all leads trimmed after soldering state **shall** either be reflowed or visually inspected at 10X to ensure that the original solder connection has not been damaged or deformed. If the solder connection is reflowed this **shall** be considered part of the soldering process and **shall not** be considered rework. This requirement is not intended to apply to components that are designed with a portion of the lead intended to be removed after soldering.

If the solder joints are found fractured after the lead trimming operation, the boards may then be fluxed and resoldered using a normal wave soldering system. This reduces the possibility of damaged joints due to lead stressing and solder coats that cut the ends of the leads. Adequate fixturing must be used to maintain board flatness through the cutting system.

11.1.3.1 Machine Soldering By definition, mass soldering implies creating many solder joints or interconnections simultaneously in a semiautomated or automated process. Equipment designed for this task generally has four basic components: product conveyance, fluxing capability, preheating capability and a standing molten pot of solder. The differences between manufacturers are typically in the application of these basic concepts and the controls of the equipment. Although each is unique, they need to be evaluated to determine the correct choice for any application, whether it is related to product size, component density, volume/capacity, or equipment service and maintenance.

Wave soldering systems are commonly used for the mass soldering of PTH and SMDs (chip and leaded devices). When bottom-side SMDs are soldered, they are typically secured with an adhesive and cured in place prior to soldering. These adhesives are specially formulated to have high ‘‘drop’’ heights (to bridge from the PWB surface at temperature +260° C). Post solder characteristics are generally limited to being nonionic, with post solder application strength being redundant to the solder connection and generally unspecified.

The wave soldering system automatically performs the soldering process, as described for hand soldering, which is flux application, heating of the area to be soldered, application of molten solder and solidification. As all of these components act together to ensure proper solder, a solder ‘‘schedule’’ is often developed by recording the optimum process parameters selected for flux, preheat, conveyor speed, solder temperature and the solder wave configuration used (on certain systems).

The ‘‘solder schedule’’ often records the preheater settings (preheater temperature and conveyor speed) vs. a thermal profile developed by placing a thermocouple on the surface

of the PWA during soldering. In order to maximize repeatability within and between PWA designs, the thermocouple is generally placed on the surface of the laminate (as opposed to the circuit trace or part lead).

11.1.3.2 Hand Soldering The use of an operator in the soldering process increases the variability of the process. A well-trained soldering operator can produce consistent and reliable quality hardware. The process engineer can provide support by making a careful hand soldering tool selection, which is properly matched to the connections being soldered.

Regardless of the soldering iron type, successful hand soldering depends on the following conditions:

• Good thermal contact between the soldering iron tip and the item to be soldered. This includes ensuring that the tip is clean and free of oxides and ''bridge'' of molted solder from the tinned tip of the soldering iron to the item to be soldered.

• Allow the flux (typically from cored solder wire or liquid flux) to flow over the area to be soldered in advance of the molten solder. The flux increases the ability of the surface to accept solder and acts as thermal transfer medium to aid in heating.

• Apply adequate solder to form an acceptable solder connection.

• Maintain thermal contact until good solder spread is obtained (but do not stay too long).

• Remove the soldering iron but do not disturb parts until solder solidification is complete.

11.1.3.3 Conforming Material Conforming sponge-like material can be used to hold components in place during wave soldering. These materials have obvious disadvantages: fabrication, cleaning, removal and frequent replacement. ''Bean bags'' or other weighty self-conforming substitutes can be used.

Web-like materials are available for spraying on the top surface of the printed board assembly. These set up on contact and are removable with water or solvents.

Too heavy an application of the ''web-like'' material can prevent the flow of the solder along the component lead and thus result in a lack of a solder fillet on the component side of the board.

Blister pack, or skin pack, is sometimes used to hold components in place during lead trimming and soldering. This method employs a transparent (sometimes bubble) sheet of plastic.

By means of a blister-packing machine, the application of heat and vacuum forms a sheet of plastic over the tops of the components and around edges of the printed board assembly. Excess plastic is trimmed from the bottom of the board before lead trimming and wave soldering. While the board is still warm, the plastic is removed.

With the blister pack process, sometimes the plastic material softens and melts during the soldering operation and it then adheres to the components leads, making it difficult to remove.

11.1.3.4 Heat Sinking Excessive exposure time and temperature can cause damage to heat sensitive parts. Thermal shunts or heat sinks, as illustrated in Figure 11-2, should be used, as required, for the protection of heat sensitive parts. They should be made of a material with good heat conductivity (e.g., copper) and the size and shape should provide adequate thermal protection and minimum mechanical interference during the soldering operation.

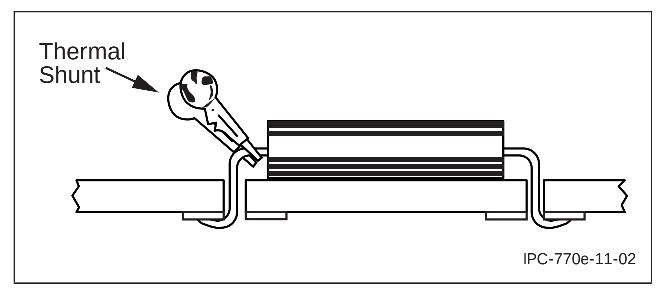


Figure 11-2 Thermal Shunt

11.1.4 Lead Termination after Assembly The objective of lead termination is to electrically connect the lead to the conductor so that the required circuit continuity is provided through the life of the equipment regardless of the environments to which the assembly may be subjected. See Figure 11-3 for examples of frequently used methods.

Leads may be attached to unsupported printed conductor lands by clinching or straight-through (unclinched) lead attachment. Soldering should complete the attachment (see Figure 11-3 B, C, D, G and H).

The component attachment should allow the lead or terminal pass through the board and be soldered to the conductor lands on the opposite side of the board.

When deciding between clinched or straight-through attachment, lead attachment should be an option with the following restrictions:

• If using flat swaged eyelets (unfused), use a clinched lead attachment.

• The diameter of unsupported holes should not exceed the diameter of the inserted lead by more than 0.5 mm for straight-through attachment.

• The inside diameter of the supported hole should not exceed the diameter of the inserted lead by more than 0.7 mm when attaching straight-through lead to supported holes.

• Leads should be terminated in such a manner that they do not exert a force on the copper foil terminal area or conductor.

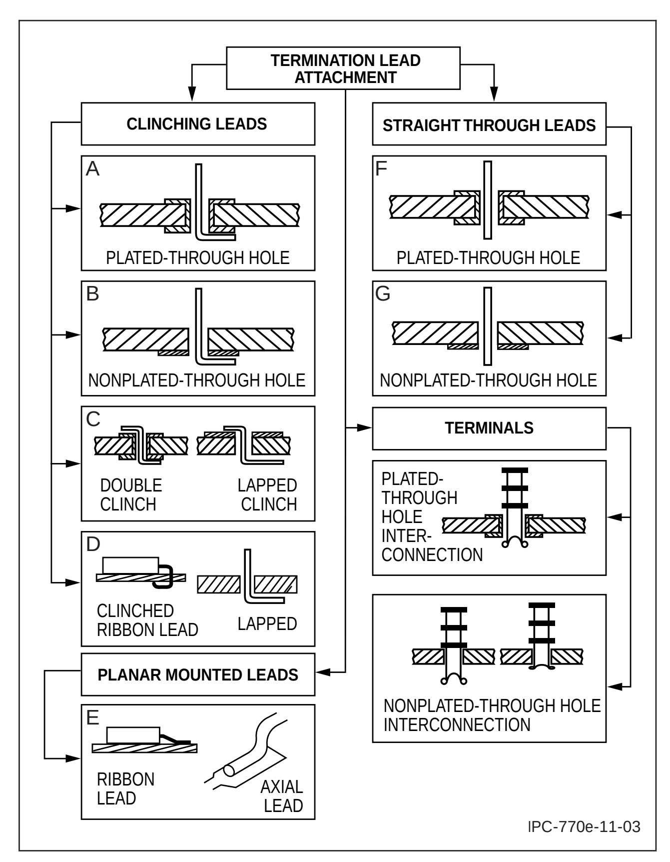


Figure 11-3 Termination Examples

- Each functional lead should have an associated terminal area.
- There should be no more than one lead in any lead mounting hole.

11.1.4.1 Unclinched Leads The most direct method for mounting components to the printed board is the straight through method with unclinched leads.

The use of straight-through unclinched leads requires minimal device handling. For example, a straightening of the component leads and cutting the leads to length before or after insertion.

The disadvantages associated with this approach are:

- The device is subject to movement both before and during the soldering operation. This makes it difficult to control the component height off the mounting surface. This movement can be a source of solder joint problems.
- It is difficult to maintain a suitable clearance between the body of the component and the printed board surface for flux removal and, when applicable, conformal coating of the assembly. This is greatly minimized when multiple lead TO cans with integral standoffs are used creating a component seating plane below the surface of the TO can from which the leads emerge.
- When the leads are rigid, precise drilling of the component mounting hole pattern is required due to small lead circle and the inflexibility of the unformed leads.
- Supported holes are preferred to enhance the mechanical strength of the solder joint. Otherwise, the clearance between the component lead, the hole and the circumscribing land must consider the lead-to-hole ratio and the hole-to-land difference. These would allow the remaining conductors to sufficiently promote solderability.
- The automatic insertion of the device leads in limited space can present problems.

The mounting of multilead component TO cans with plastic spacers has been used to overcome some of the disadvantages for the more conventional straight-through lead mounting techniques. Spacers with protrusions on one side should be mounted with the protrusions against the board. In addition to the considerations common to the straight through mounting techniques, mounting of the components with spacers has the following advantages:

- Suitable clearance between the component body and the printed board can be maintained to facilitate soldering flux removal and conformal coating.
- Bearing surface for the body is provided if the component leads are to be clinched.
- The extension of unclinched leads beyond the printed board surface can be more accurately controlled.
- The height of the component body above the printed board surface can be more accurately controlled. This is especially important when the printed board assemblies are closely spaced.
- The spacer helps to reduce the magnitude of mechanical stresses that are transmitted to the lead/body interface seal.
- The lead mounting hole pattern need not be held as accurately as for not preformed component leads.

The use of spacers has the following additional disadvantages:

- Additional cost.
- Increase in the amount of assembly labor.

11.1.5 Preformed Leads Offset multilead mounting methods have been developed to overcome the restrictions of small component mounting holes and their associated small hole and land diameters with little or no space for conductors between the leads. When the components are removed from the forming die, the packages are usually hand-assembled and clinched to hold them in place. Spacers are available for units with press-on heat sinks or formed leads that have to be kept off the board. The following lists considerations of using the offset multiple lead mounting method without clinched leads:

- Allows for larger lands and component lead holes.
- Requires less stringent board fabrication tolerances, if desired.

- May be used with conductors that can be routed between lands.
- May reduce (circular pattern) or eliminate (rectangular pattern) the number of off-grid mounting holes and lands.
- Can provide the needed spacing for flux removal and conformal coating.
- Requires considerably more mounting labor and usually tooling or fixturing.
- Care must be taken to assure that the lead forming process does not unduly stress the lead/body interface seal.

Takes up more printed board area by the component-mounting pattern.

- Preformed leads can also be used for mounting components off the board.
- Preformed leads can reduce stress on land board patterns on single sided boards.

11.1.6 Component Retention

11.1.6.1 Clinched Leads Clinching of leads prior to soldering is commonplace, either as part of machine insertion or following hand insertion. The substrate land configuration and spacing to adjacent lands must be considered. Clinching in line with traces is good practice and trimming of leads before clinching is recommended where clinch direction may cause shorting to adjacent lands. It is generally not felt to be necessary to clinch all leads of a multi-leaded device unless required by the customer. The lead or terminal should make contact with the conductor pattern before soldering. Leads should not extend beyond the edge of their lands, however, if overlap does occur, the lead should never violate electrical spacing requirements. Eyelets may support the lead termination hole or plated-through-holes. The holes may also be unsupported.

The lead should be cut and clinched prior to the soldering operation (see Figure 11-4).

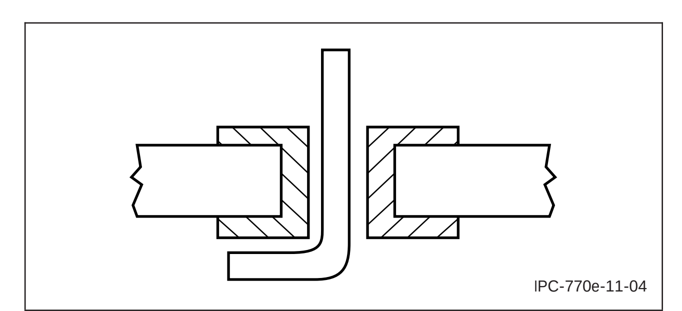


Figure 11-4 Clinched Lead

As its name implies, the component leads for this method are clinched to the printed board land after they have passed through the lead hole.

In addition to the considerations common to all straight-through mounting methods, this method has the following advantages:

- A reinforced mounting hole is not required; teardrop and offset lands can be used.
- Some resistance to movement during soldering is afforded.

This method has some of the disadvantages mentioned for unclinched straight-through mounting, in addition:

- Care must be taken when cutting the lead to length and forming the clinch to assure that minimum conductor clearances are provided when the clinched lead overhangs the land.
- The lead clinching operation, if not controlled properly, can unduly stress the component lead-to-can body seal.
- The method and means chosen for component retention should take the following factors into consideration.
- End use of assembly and possible need for repair; component removal, replacement and soldering without damage to the printed boards, plated-through-holes and/or lands. Straight through leads are the simplest in this respect.
- Stresses on leads at the junction of the component body, especially for hermetically sealed or glass bodied components.
- Allowable distance from the bottom of the printed board to the end of the component leads, and desirable solder fillet.
- Area and direction available for clinching or bend-over without danger of proximity to other leads or conductors which may result in shorts or solder bridges.
- Possibility for internal voids and entrapments of flux gases, etc., if leads are curved and bent inside the hole contacting hole corners.
- Hazards to personnel created by sharp or knife-like lead ends.
- Potential for fractured solder joints when leads are cut after soldering.
- Potential for lifted lands.
- Requirement for lead ends to be covered with solder.
- Applicable specification constraints on component retention techniques and results.

Axial lead forming is normally along the centerline of the component and inward, back toward the body. The clinch is either 90° or 45° (see Figure 11-4). The clinch lead length (L) of the component lead under the printed board is a function of the lead diameter, as shown in Table 11-1 and Figure 11-5.

Note: The clinched lead length is measured parallel to the printed board, after clinch.

The clinch length for the normal 90° clinch pattern is measured from the centerline of the component lead as it extends through the hole in the printed board. The minimum clinch lengths for small diameter leads are somewhat

Table 11-1 Lead Clinch Length

Wire Diameter	Minimum Clinch	Maximum Clinch
0.5 mm [0.20 in]	0.8 mm [0.030 in]	2.0 mm [0.080 in]
0.8 mm [0.030 in]	1.0 mm [0.040 in]	2.0 mm [0.080 in]
1.0 mm [0.040 in]	1.3 mm [0.050 in]	2.0 mm [0.080 in]
1.3 mm [0.050 in]	1.5 mm [0.060 in]	2.0 mm [0.080 in]

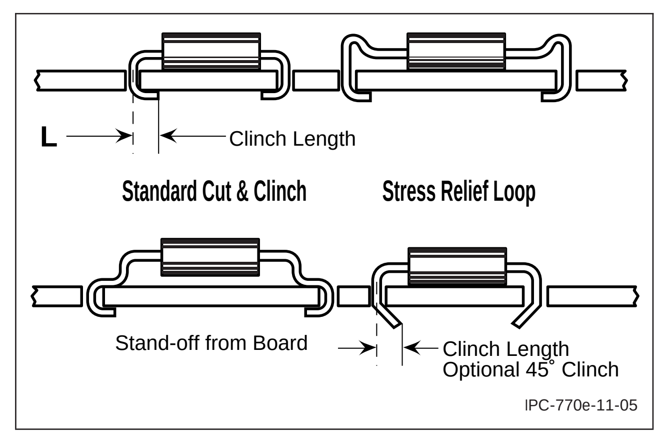


Figure 11-5 Clinch Patterns

dependent on the hole diameter in the board. To maintain a minimum clinch length, the hole size must not be more than 0.36 mm larger than the component lead diameter.

When printed boards are drilled to close positional tolerances with minimum recommended hole sizes, the 45° clinch length, dimension ‘‘L,’’ may be as small as 0.8 times the lead diameter. This allows only 0.3 times the lead diameter extending over the land. In this case, two wire diameters should be allowed for the distance below the board.

Use of automatic insertion machines provides a built-in means for holding of components. (For most reduced reliability applications, the components need not be retained rigidly in position during wave soldering.) Numerically controlled insertion equipment provides for accurate placement of components (if tape sequence and program are correct). Inspection of automatically inserted components is usually through a sampling plan and/or a first article inspection to check out the tape sequence and program.

11.1.6.2 Offset Clinch A slight modification of the mounting method just described is the offset multiple lead mounting method with clinched leads. As shown in Figure 11-6, this method adds the leads clinched to the conductor land after they pass through their mounting holes.

11.1.6.3 Semiclinched Leads The lead is passed through a hole in the board, cut to length and soldered. When straight-through leads are used in conjunction with unsupported holes, the leads should extend from 0.5 mm minimum to 1.5 mm maximum from the surface of the foil.

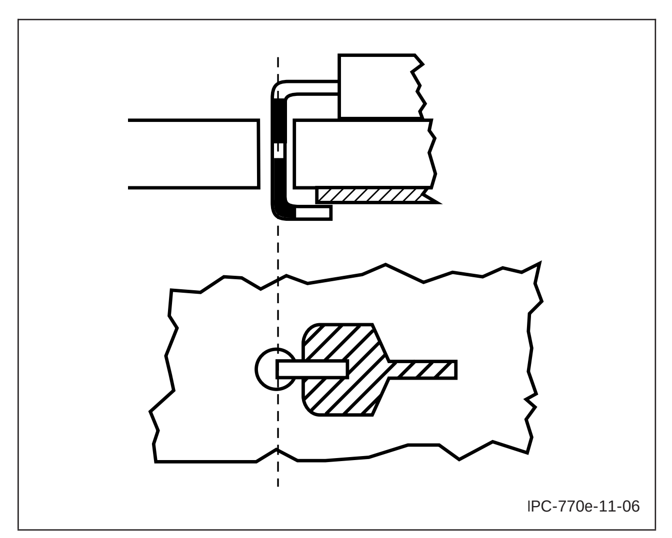


Figure 11-6 Offset Clinched Lead

When straight-through leads are used in conjunction with plated-through holes or eyelets, the lead should extend at least to the surface of the plating or rim of the eyelet and no more than 2.3 mm from the plating surface eyelet. Semiclinched leads should be considered as straight-through leads providing the degree of clinch meets the requirements shown in Figure 11-7.

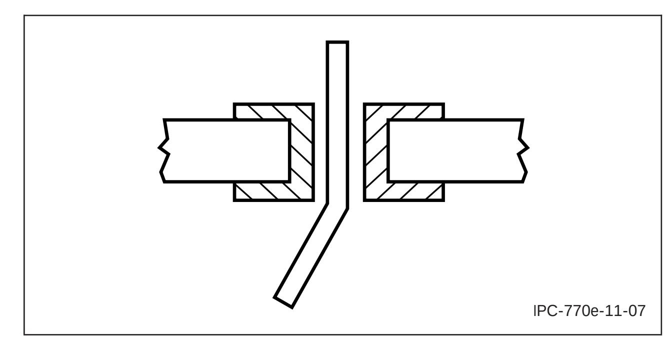


Figure 11-7 Semiclinched Lead

11.1.7 Lead Cutting Cutting of component leads may be accomplished manually or by automated equipment. When automated lead cutting is used, it is usually necessary to retain the parts on the board during the cutting process. Leads may be cut either before or after soldering. However, cutting leads after soldering requires that cutting methods, sharpness of cutting tools, lead material, or procedures are such that they do not induce solder fractures. Some specifications require that the leads clipped after soldering be reflowed to insure the integrity of the solder joint or require the 100% of the solder connection at 10X. The retention method may also serve to retain the parts during a second soldering operation.

As with any cutting instrument, as blade usage on the automatic lead cutter increases, cutting quality diminishes. In some instances, the small lead section is not entirely removed from the lead leaving a ‘‘flag’’ or ‘‘lid’’ attached to the lead end.

Surface mount components mounted to the bottom side of the board may also interfere with the lead cutting operation.

11.1.8 Axial Leaded Component The lead should extend approximately one lead diameter out from the body of the component. This spacing radius is usually expressed as ''lead diameters'' or a minimum of 0.8 mm [0.03 in] prior to the start of the bend. The end of the body in this application is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension. See Figure 11-8 to view the minimum component center-to-center board lead spacing.

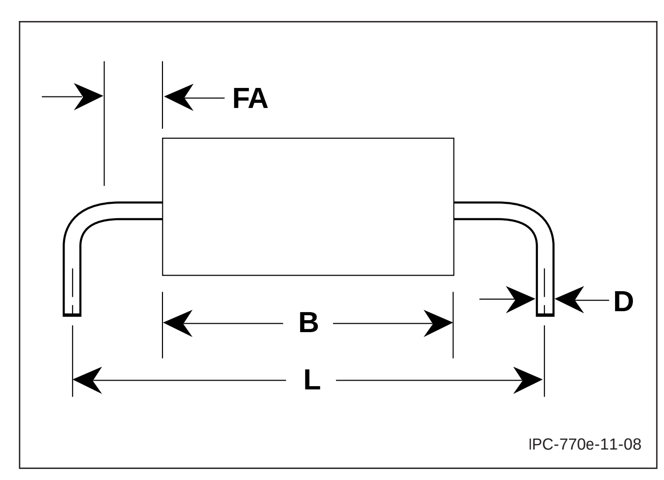


Figure 11-8 Bend Configuration

It can be represented by the following equation:

C/C = B max + 3D* + 2 L

where:

- C/C = Center to center lead spacing
- B = Body length
- D = Nominal lead diameter
- L = Forming allowance (lead should not be disturbed within this distance from the body)
- L = or 0.8 mm whichever is greater

*For lead diameters up to 0.8 mm, 4D for lead diameters between 0.8 mm and 1.2 mm and 5D for lead diameters over 1.2 mm.

The value of ''C/C'' is usually adjusted upward to coincide with the grid used. The total length of both leads should not exceed 25 mm in length unless this component is mechanically supported to the mounting base.

11.1.8.1 Minimum Inside Bend Radius The minimum inside bend radius of a single 90° bend of a component lead should be in accordance with Figure 11-9.

11.1.8.2 Stress Relief Properly formed leads on axial-leaded components normally afford adequate stress relief when formed as shown in Figures 11-8 and 11-9. Mechanically sensitive components, such as glass diodes, may require other relief configurations and have one or more leads formed with a stress loop/bend to conform to requirements stated in the paragraph above. Whenever the possibility exists of solder wicking into the relief bend as a result of a small diameter component, alternate stress loop/bend configurations in or spacers should be provided as the stiffened lead defeats the purpose of the relief (see Figure 11-10).

11.1.8.3 Lead Forming for Component Retention The purpose of preforming component leads is for retention to the board during the wave solder operation or to have the components elevated off the board per the product requirements.

The forming of leads can be from as minimal as a simple offset to as complex as a compound form. The major factors affecting the forming of leads are board thickness, lead diameter, lead material, hole size and tooling required.

11.1.8.4 Simple Offset Method Figure 11-11 illustrates a component with a straight through lead. The advantages are ease of forming and insertion. The disadvantage of this forming is a minimum of retention force and the resiliency of small or soft component leads.

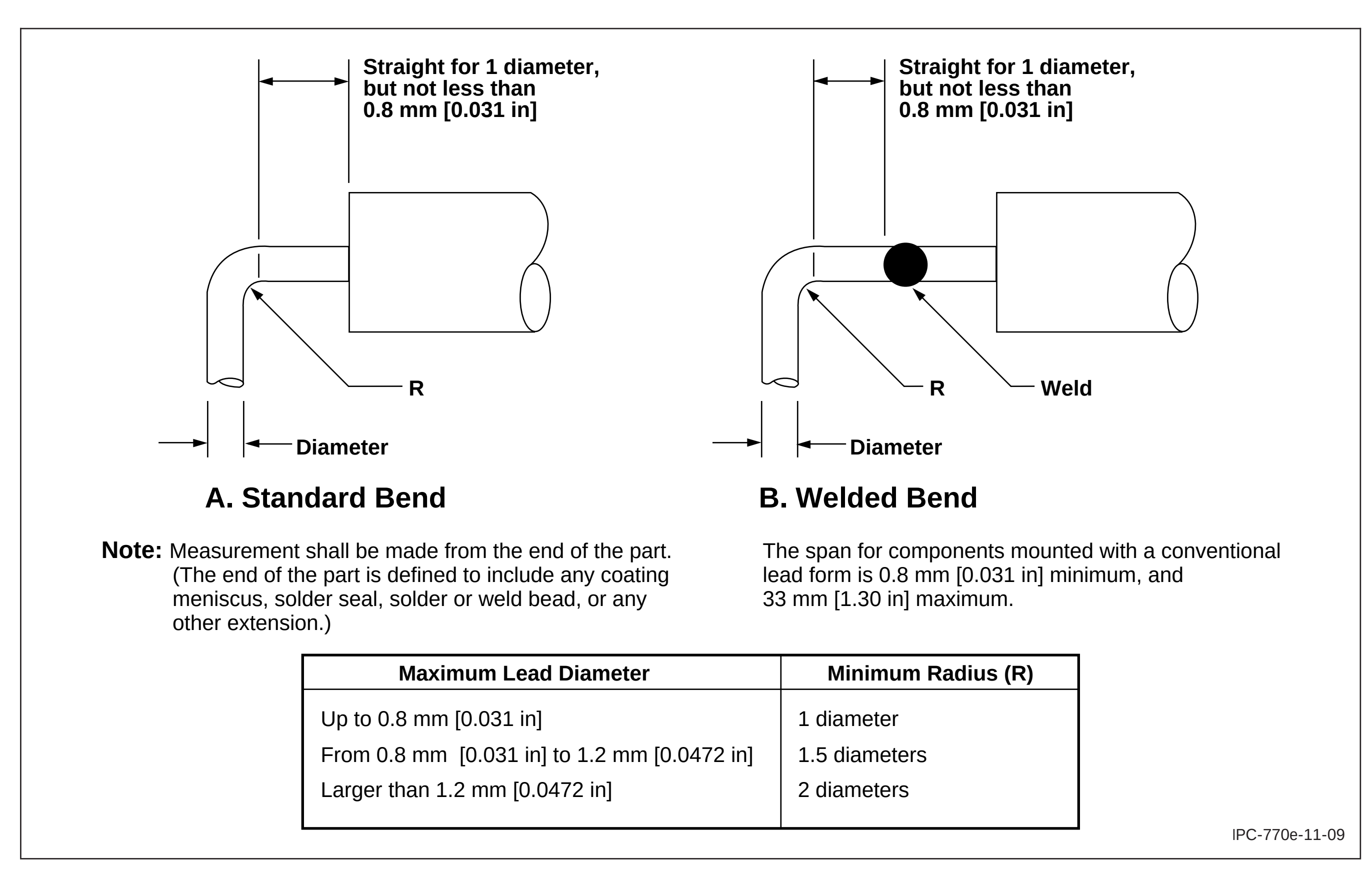
11.1.8.5 The Dimple This method increases the retention of the component to the board and gives better contact to the board circuitry. The main disadvantages are the die sets required to form the leads and the hole size to dimple height requirements. (see Figure 11-12).

11.1.8.6 Compound Forms This method gives the best retention and has the advantage of clinched lead reliability. Disadvantages include complex tooling required to form leads and the need for consistent hole-diameter tolerances (see Figure 11-13).

11.1.8.7 Combinations of Forms These are used to gain the advantages of the above methods and overcome some of the disadvantages (see Figure 11-14).

11.1.9 Radial Leaded Discrete Component

11.1.9.1 Component Preparation Under certain circumstances, it may be advisable to provide stress relief for the leads of radial-lead components by forming the leads outward from the normal component lead pattern to an enlarged pattern. Another method of providing stress relief for radial-lead components is the use of a flexible low-modulus spacer supported by rounded protrusions (see Figure 11-15).



Maximum Lead Diameter	Minimum Radius (R)
Up to 0.8 mm [0.031 in]	1 diameter
From 0.8 mm [0.031 in] to 1.2 mm [0.0472 in]	1.5 diameters
Larger than 1.2 mm [0.0472 in]	2 diameters

Figure 11-9 Lead Diameter Versus Bend Radius

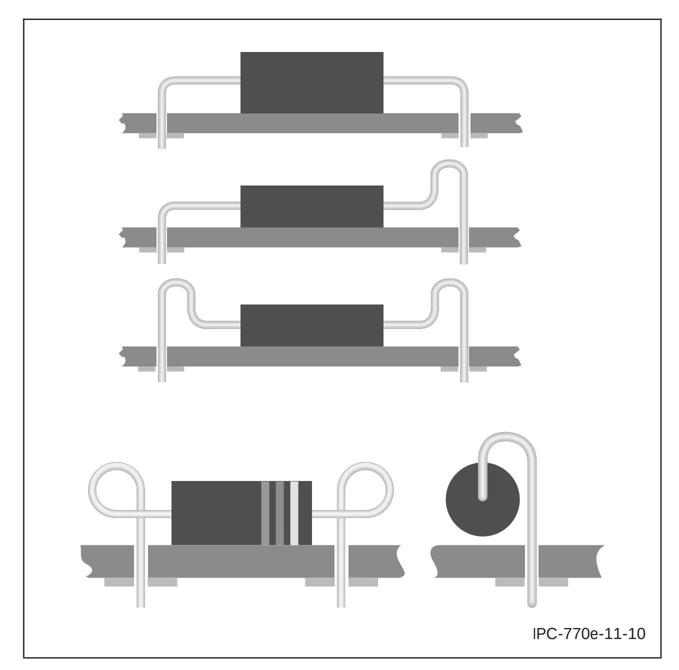


Figure 11-10 Stress Relief Examples

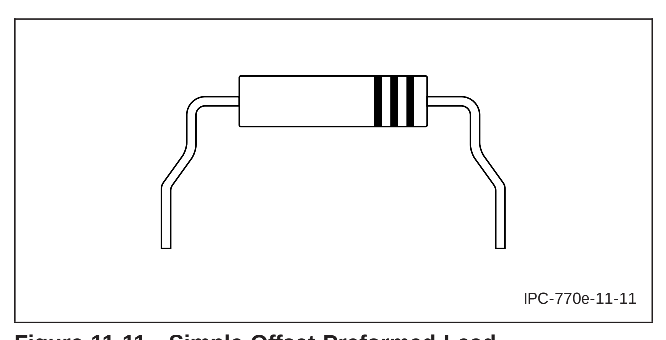


Figure 11-11 Simple-Offset Preformed Lead

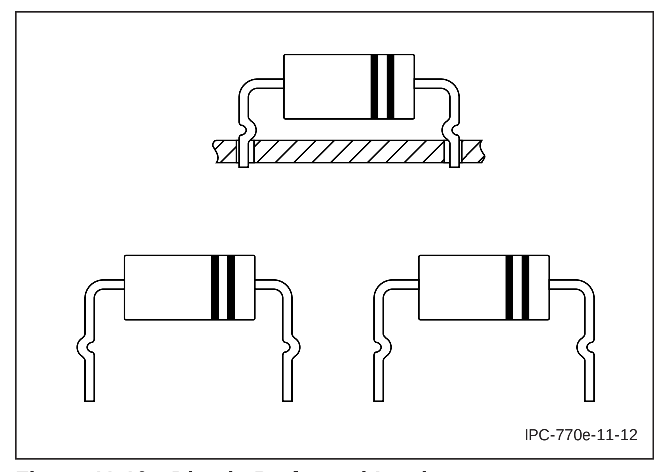


Figure 11-12 Dimple Preformed Leads

11.1.9.2 Multiple Radial Lead Components Multilead TO cans are used in many printed wiring assembly applications. However, the wide variety of multilead TO can sizes and the varying number of leads make it impossible to standardize on a mounting method. This section dis-

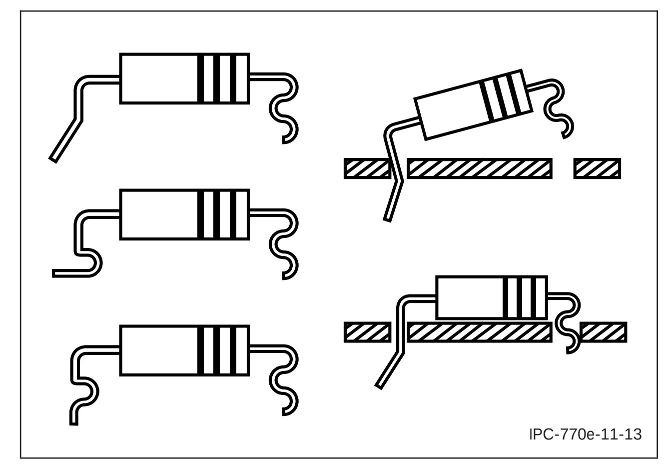


Figure 11-13 Compound Preformed Leads

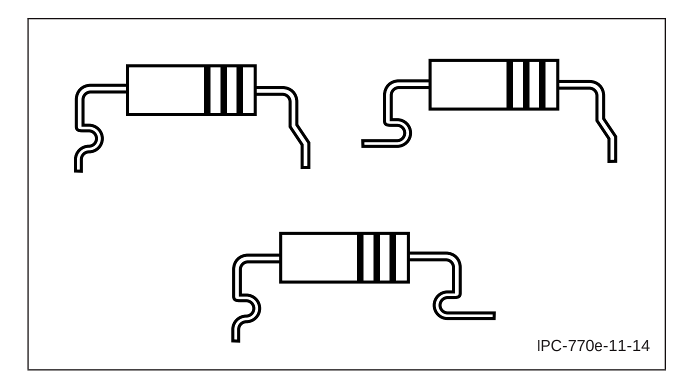


Figure 11-14 Combination Preformed Leads

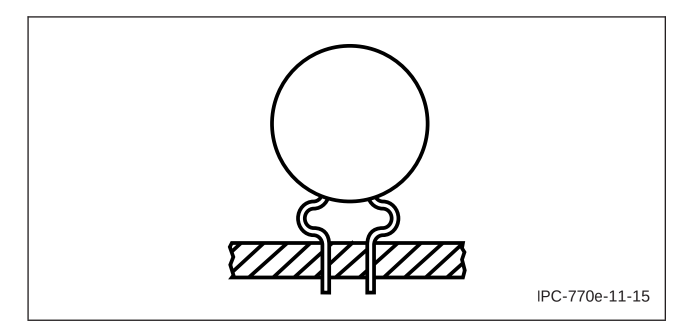


Figure 11-15 Stress Relief Leads

cusses the more commonly used multiple-lead TO can mounting techniques.

11.1.9.3 Lead Forming Leads exiting from multilead radial type components may be formed to standard grid spacing by forming the leads to a larger pattern from beneath the component body. This technique is used to provide inspection of solder joints, stress relieving component leads, enhanced cleaning, etc., as shown in Figure 11-16.

11.1.9.4 Component Retention The dimple in Figure 11-17 increases the retention to the board and gives better contact to the board circuitry. The main disadvantages are the die sets required to form the leads and the hole size to dimple height requirements.

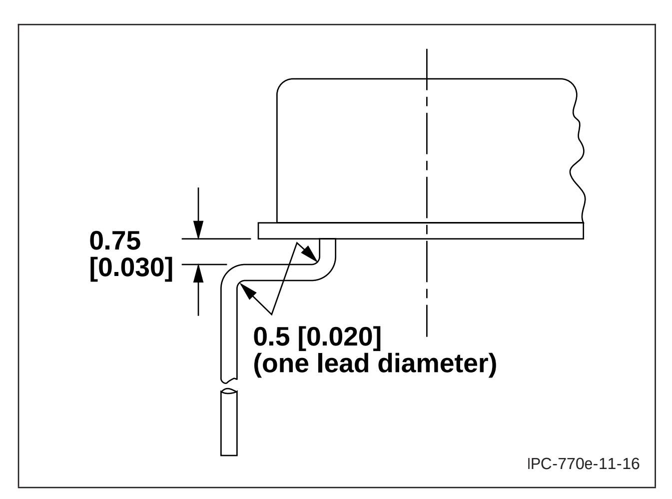


Figure 11-16 TO Can Lead Forming

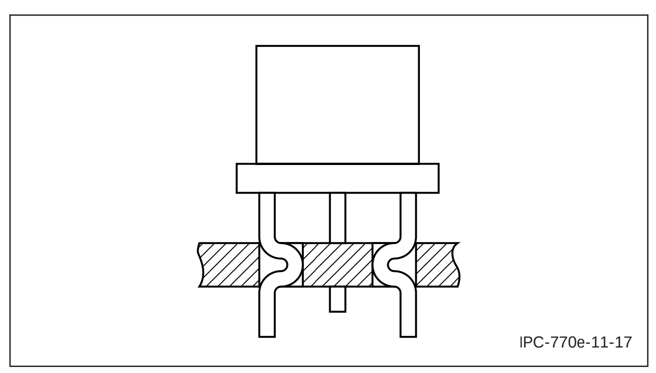


Figure 11-17 Dimple Preformed Leads

11.1.9.5 Lead Configuration after Assembly The basic multilead TO can mounting techniques can be grouped as follows:

- Straight-thru lead, unclenched.
- Straight-thru lead, clinched.
- Straight-thru lead, with spacer (clinched, unclinched).
- Preformed lead, unclenched.
- Preformed lead, clinched.
- Preformed lead, with spacer (clinched, unclinched)

A mounting pattern for 12 1ead multiple-lead TO cans with radially offset and clinched component leads, such as TO-73 and TO-101, is shown in Figure 11-18.

11.1.10 Mechanical Securing A method for mounting of a transistor that must be mechanically secured to the surface of the board is shown in Figure 11-19.

11.1.11 Inline Leads The mounting pattern shown in Figure 11-20 employs ''inline'' leads and lands for through hole mount devices. Although such inline lead arrangements simplify lead-forming requirements, they result in very closely spaced lands (approximately 0.8 mm clearance) and therefore require the use of close tolerance manufacturing processes for fabrication and assembly, particularly for through-hole mounting.

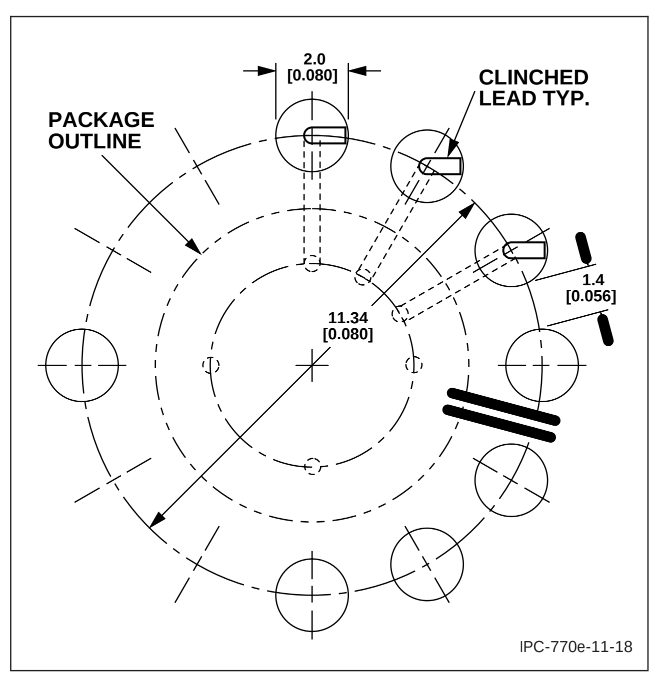


Figure 11-18 Typical Mounting Pattern for 12-Lead Cans with Clinched Leads Mounting

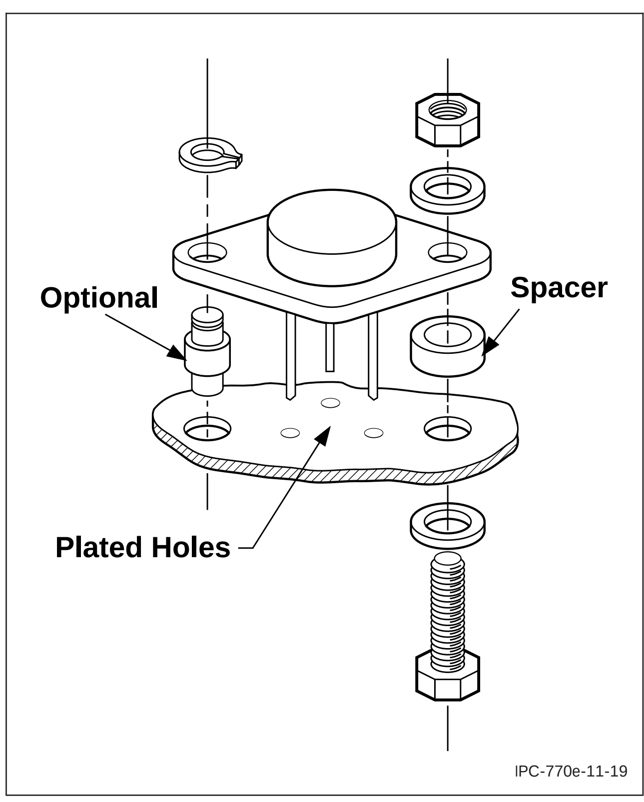


Figure 11-19 Mechanically Secured Transistor

A disadvantage of the inline arrangement is the limited space available for conductor routing between terminal areas.

11.1.11.1 Single-Inline Package (SIP) These components are ready for manual insertion without the use of special tools or fixtures. Lead preparation is not normally required. Lead clinching is required to the board for component retention through manufacturing operations. Standoffs are usually built into the component body to accomplish proper board spacing as shown in the typical SIP specification in Figure 11-20.

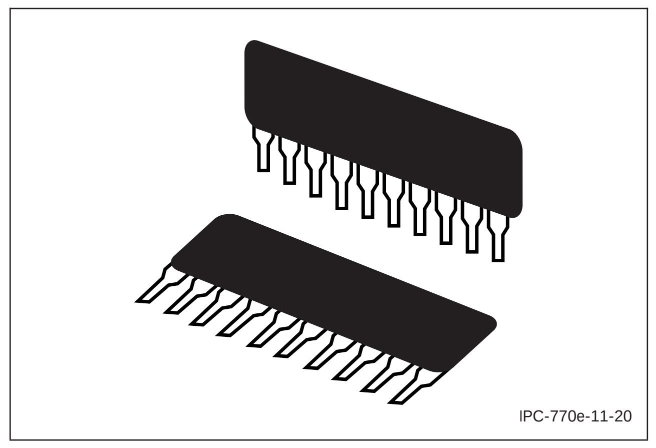


Figure 11-20 Single-Inline Component

11.1.11.2 Dual-Inline Package Dual-Inline Package (DIP) packages (whether printed board lands are of a round, square or ribbon across section) leads should be dressed to and through the printed board.

The maximum clinched lead length is dependent upon the length of lead that is available for cutting and clinching and the thickness of the printed board. In all cases, the land diameter should be large enough to accommodate the clinched lead to minimize solder bridging. A minimum of two (2) leads on opposite corners should be clinched for part retention as shown in Figure 11-21.

The base of the device should be parallel to the surface of the printed board to the extent that minimum lead protrusion and maximum component body height from the board is maintained (see IPC-A-610).

Heat sinks, when required, should be properly secured so that they do not stress the subsequent solder joints. A resilient spacer may be used as shown in Figure 11-22.

The lead-to-body seals of mounted devices must be undamaged. Body chipouts that extend to or into the glass seal; chipouts that expose a normally encased area of a lead, and hairline cracks in either the seal or the body are not acceptable.

11.1.11.3 Staggered Leads Other disadvantages associated with inline patterns can be overcome by the use of ‘‘staggered’’ lead arrangements (see Figure 11-23). In these mounting patterns, a convenient distance from the inline axis offsets the lead hole and lands of adjacent leads on the same side of the flatpack. Lead forming is normally accomplished using fixed dies, which bend all leads simultaneously and uniformly. Although a staggered lead arrangement requires somewhat more board area per device than

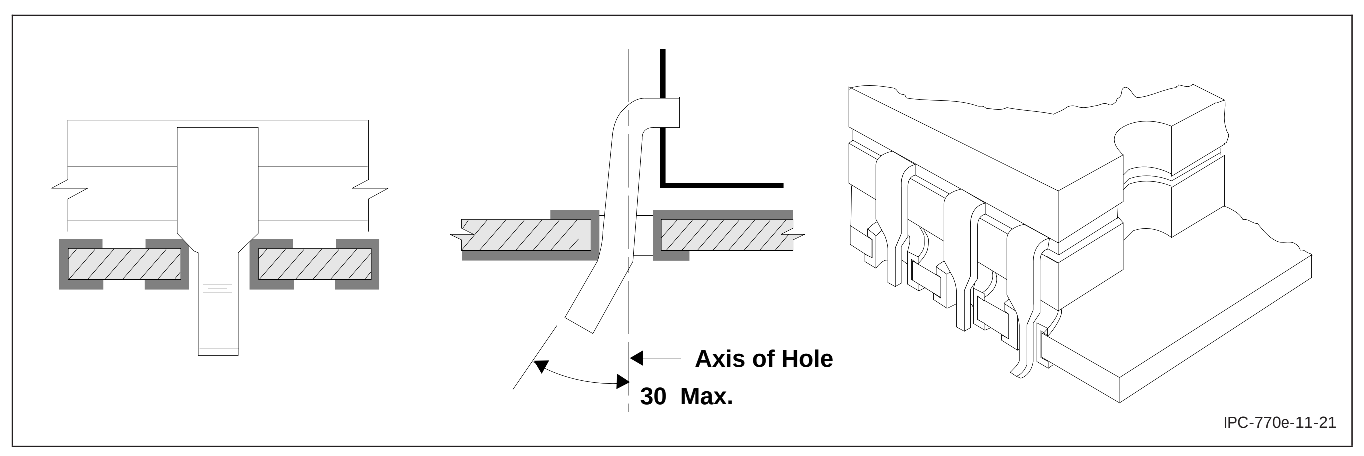


Figure 11-21 Lead Configuration (After Assembly)

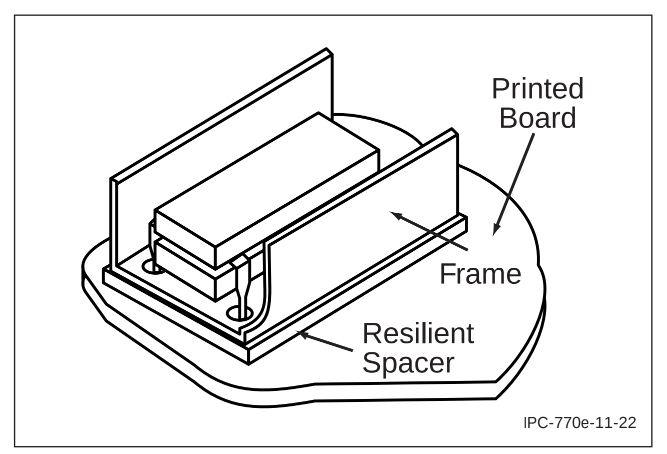


Figure 11-22 Resilient Spacer to Heat Sink Frame

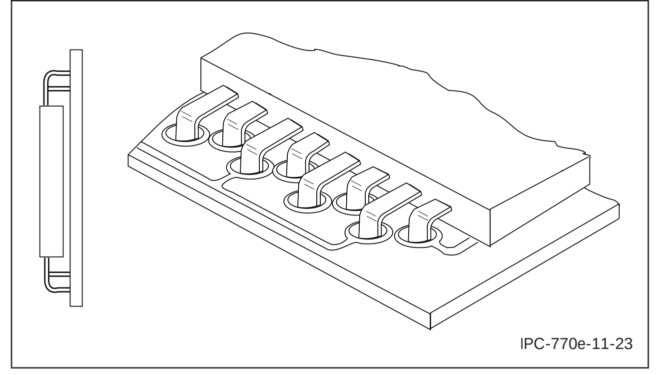


Figure 11-23 Staggered Hole Pattern Mounting (Flatpack Outline Drawing)

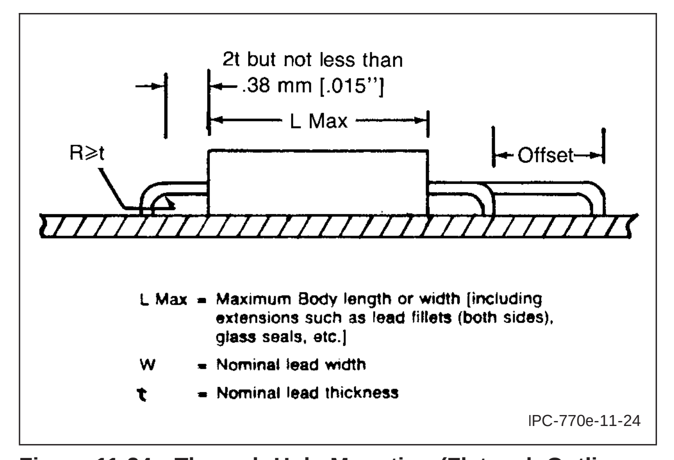


Figure 11-24 Through-Hole Mounting (Flatpack Outline Drawing)

the inline arrangement, it provides several of the following advantages:

- Tolerances are less critical.
- Larger lands can be used.
- More space is available for routing conductors between adjacent lands.
- Larger component lead holes can be used to simplify component insertion.

In the staggered lead arrangement a good compromise between loss of available board area and the increase in the number of through conductors can be achieved by the use of a 2.5 mm offset between adjacent land area. With this arrangement, conventional manufacturing tolerances are applicable, and a 0.25 mm annular ring (a practical minimum) is possible. The maximum offset that can be achieved with flatpack leads of 6.4 mm length is 3.8 mm. When this maximum offset is used, only the through-hole (unclinched leads) type of mounting is practical.

Hand held tooling is also available to bend all leads on one side of the device. All tooling should protect the device seals by supporting the lead between the body and the bend. Lead bending and forming requirements for typical packages are shown in Figure 11-24.

11.1.11.4 Unclinched Flatpack Leads In the through hole flatpack mounting method with unclinched leads, the flat leads are formed at a 90° angle and inserted in mounting holes in the printed board (see Figure 11-25).

11.1.11.5 Clinched Leads Flat packs mounted in unsupported holes with annular ring should be clinched at a minimum of 45° and lead protrusion of at least 0.5 mm (see Figure 11-26).

The purposes of using this type of flatpack mounting are:

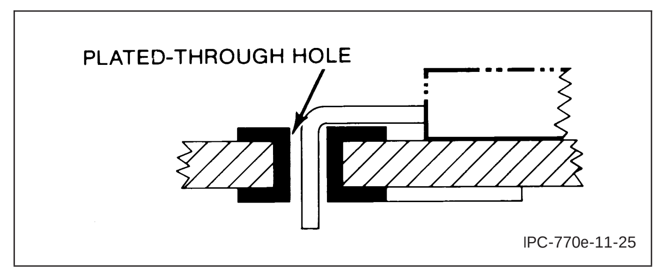


Figure 11-25 Through-Hole Board Mounting with Unclinched Leads

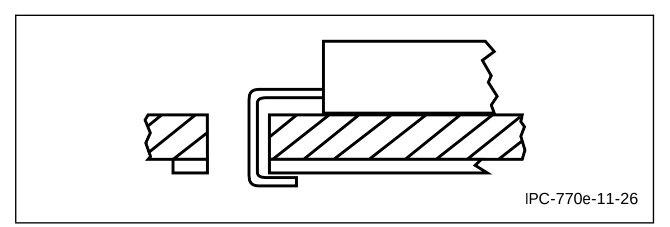


Figure 11-26 Through-Hole Mounting with Clinched Leads and Circumscribing Land

- The flatpack is positioned to withstand the forces exerted upon it during the mass soldering operations.
- The hole-to-lead clearance is not as critical.
- Solder connections are more reliable than unclinched mounting due to additional mechanical contact.

A common variation of the through-hole, clinched-lead flatpack mounting method, as opposed to the annual ring method is where the land is offset (see Figure 11-27).

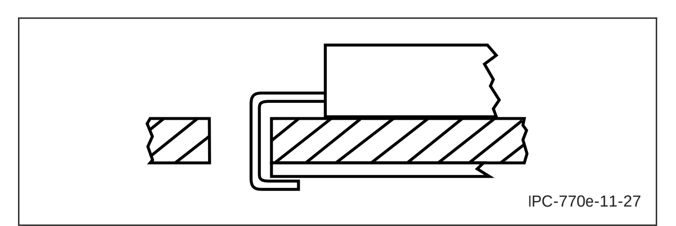


Figure 11-27 Through-Hole Mounting with Offset Land

11.1.12 Pin Grid Array Components To accommodate a high count of I/O pins, the pin-grid array package can be inserted in the present 100-mil grid through-hole process and subjected to wave soldering. However, because of the risks involved with removal of these packages, various socket styles have been utilized in this application.

Inspection of the solder connections under the package body can be easily performed on the solder side of the board and the device can be tested on existing ‘‘bed of nails’’ testers.

Inspecting the solder joints on the component side of the board is extremely difficult without the aid of special tools such as a fiber optic inspection system or a laser system where joint temperature profile is indicative of the amount of solder and integrity of the joint.

For this reason and because of the risks involved with removal of these packages, sockets have been utilized. Low profile grip sockets can also be used.

11.1.12.1 Component Preparation Lead Forming of Pin Grid Array pins is not recommended. They should be through-hole mounted with straight lead attachment.

11.1.13 Through Hole Mounted Connector Chamfered lead ends are recommended for large connectors. Lead and hole location becomes more critical as the number of I/Os increase. As in any multilead device, the true position of pattern clusters becomes critical for reliable installation and ease of manufacturing. The use of a secondary reference such as a hardware hole is recommended. Connector manufacturers should be contacted for installation aids availability.

11.1.13.1 Through Hole Mounted Socket Lead Configuration after Assembly Socket contacts are normally stationary (nonformable), preset and typically protrude through to the board surface. Stamped contacts without mechanical grip and clinching are recommended. A post assembly terminal review should highlight lead length conformance and separation of lead ends from other leads or surface conductors.

11.1.13.2 Polarization The device and socket assembly/application specifications, as well as the board markings are the principal controlling documents for orienting sockets on the board. Sockets are visually and dimensionally symmetrical and may only offer visual aids (dot, slanted corner, tab, etc.) on the part to orient it. Therefore, the controlling assembly document should note the visual aid and the pin numbers.

11.1.13.3 Lead Forming and Alignment Lead forming is not usually performed on sockets, but if it is necessary, the fixture or tool must ensure that the integrity of the contact areas remains intact, and that the lead is not deformed beyond 10% of the lead diameter.

11.1.13.4 Seating With sockets being relatively light in relation to their land patterns, some of the leads penetrating the board can be improperly seated. For example they can either be not fully bottomed out to the board or have a lead or two crushed down (beneath the body). After assembly, a visual inspection should be performed prior to soldering.

11.2 Component Placement

11.2.1 Straight Through Leads Straight through lead definition includes partially clinched leads, where the components are secured with only limited movement and the leads are in contact with the land patterns.

Lead projection from an unsupported hole should be 0.5 mm minimum. Lead bend at the solder side is allowed to extend so the minimum electrical clearances are maintained. Lead projection from a supported hole should extend at least beyond the bottom surface of the board to the extent that, as a minimum, the lead contour is discernible after soldering.

Lead projection of specially preformed leads for component retention without clinching can be used to eliminate the need for post-soldering lead cutting.

11.2.2 Clinched Leads Clinched leads are leads that are formed to the lands for both supported and unsupported holes. Leads may extend beyond the land, but should not violate minimum electrical spacing.

11.2.3 Lead Spacing Where practical, components with similar physical dimensions should have the same lead spacing and be on the design grid.

11.2.4 Component Body Through-hole components may be mounted on both sides of the board. Components should not be mounted across or on top of vias or exposed conductive patterns unless adequately electrically insulated (see Figure 11-28).

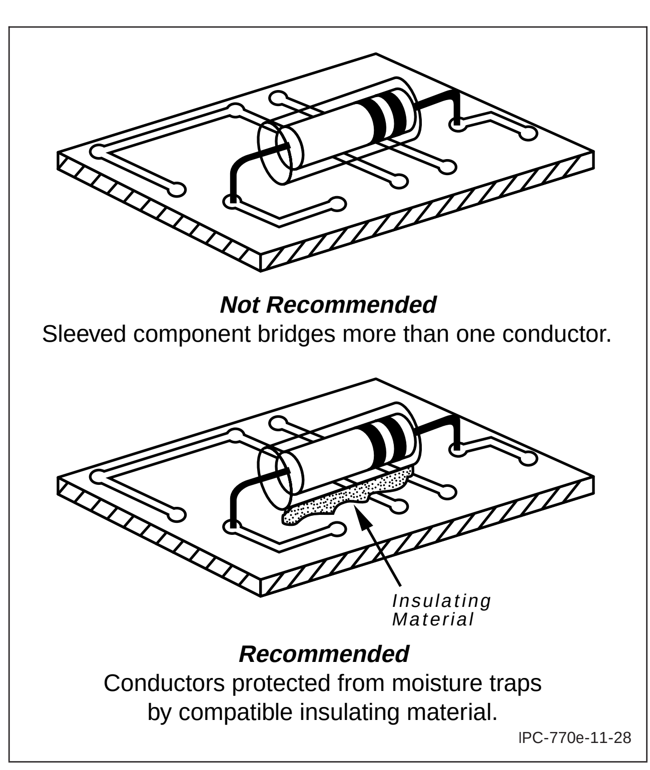


Figure 11-28 Components Mounted Over Conductors

Resistors with high heat dissipation should be mounted with a clearance of at least 1.5 mm from the board surface. Parts or metal case components mounted over electronic circuitry should be insulated from the conductive elements. Insulation materials should be compatible with the circuit and the board material. Conductive areas under parts should be protected against moisture entrapment by one of the following methods:

- Application of conformal coating using material in accordance with IPC-CC-830.
- Application of a cured resin coating by using low flow prepreg material.
- Application of a permanent polymer coating (solder resist) in accordance with IPC SM-840.

Component bodies should not be closer than 1.5 mm from the board edge.

11.2.5 Hardware Clearance Component and printed board mounting requirements should consider possible conflicts with the printed board conductor pattern, routing and density. This consideration reduces the likelihood of mounting hardware violating electrical clearance requirements (see Figure 11-29).

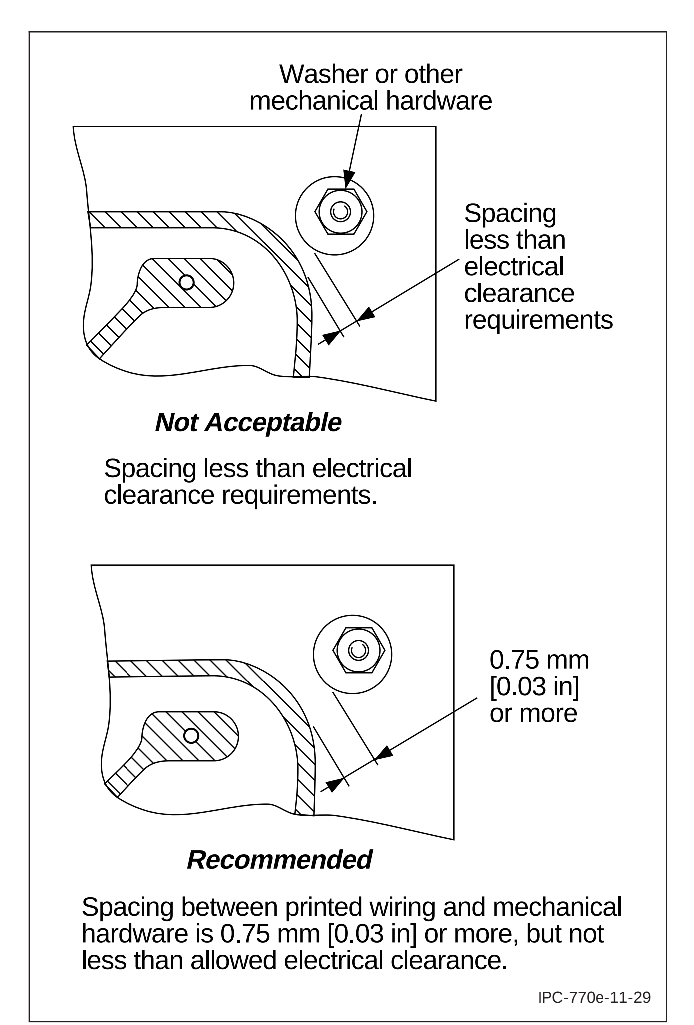


Figure 11-29 Uncoated Board Clearance

Component density placement should consider the requirements for electrical clearance, thermal dissipation, and ease of rework and repair processes. When component density

results in close and/or physical contact of components, the following requirements should be considered:

- Isolation resistance.
- Thermal dissipation.
- Reduction of component power rating.
- Reduced reliability of heat sensitive components in the vicinity of heat generating components.

11.2.5.1 Horizontal Axial Leaded Discrete Components Horizontally mounted components should be oriented in either of the two board plane axes preferably with component identification in the same direction. The body of the component should be approximately centered between the lead mounting holes (see Figures 11-30 through 11-33).

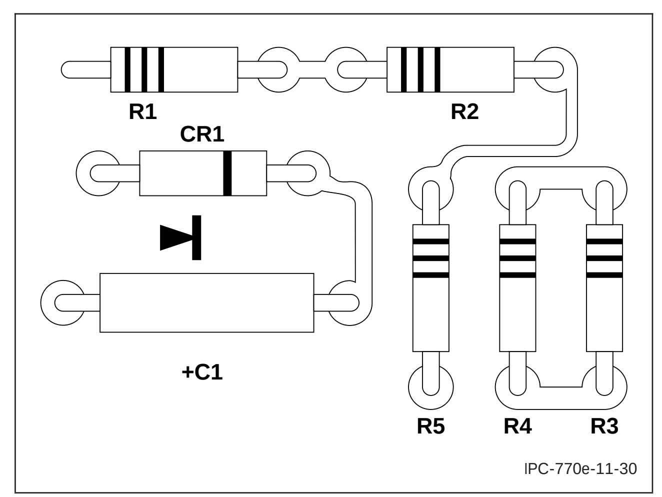


Figure 11-30 Component Alignment

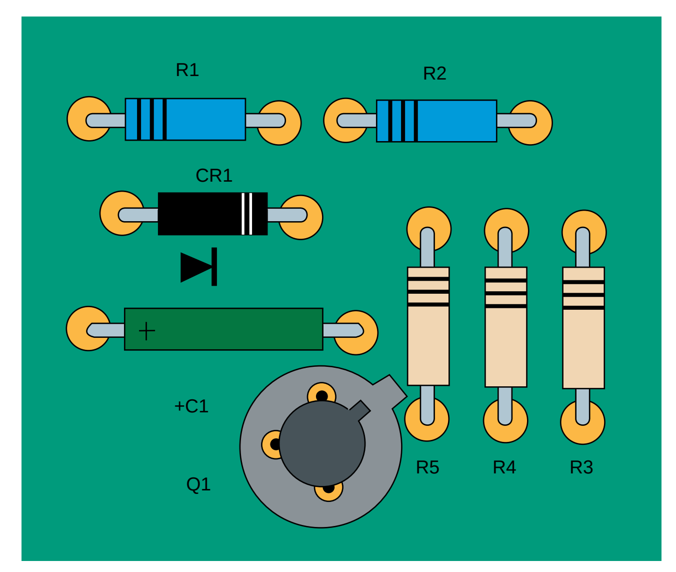


Figure 11-31 Component Alignment

The clearance between component leads or components with metal cases and any other conductive path should not violate minimum electrical spacing. Parts and components should be mounted so as not to obstruct solder flow on the topside termination areas of plated through holes that require soldering.

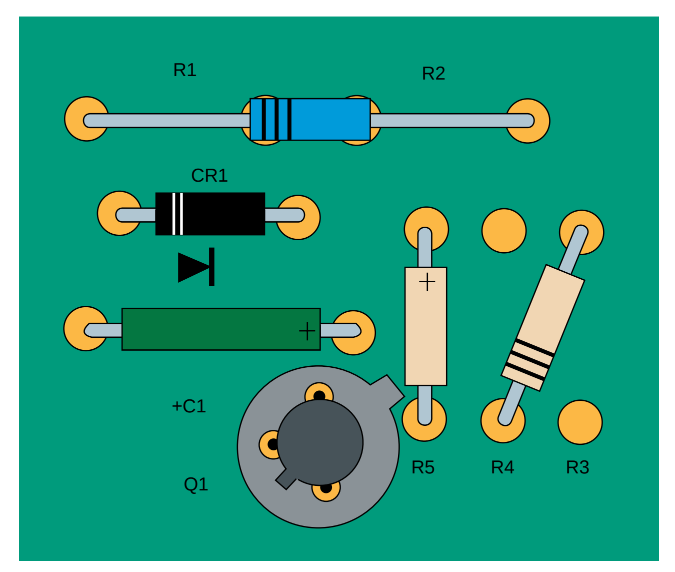


Figure 11-32 Component Misalignment

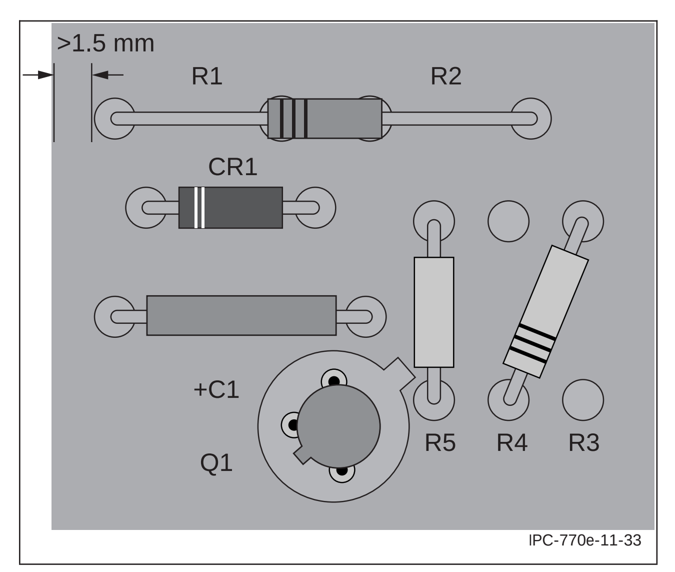


Figure 11-33 Component Misalignment Clearance

Component bodies should not be closer than 1.5 mm from the board edge.

11.2.6 Radial Leaded Discrete Components

11.2.6.1 Horizontal Mounting When radial leaded components (e.g., transistors in TO cans) are mounted horizontally, mounting clips or adhesives should be used. A typical method of mounting a component of this type is shown in Figures 11-34 and 11-35.

11.2.7 Plastic Power Transistors Plastic power transistors are designed such that the mounting hardware may also be a part of the active circuit. A typical mounting of such a device is shown in Figure 11-36. Lead bend radius

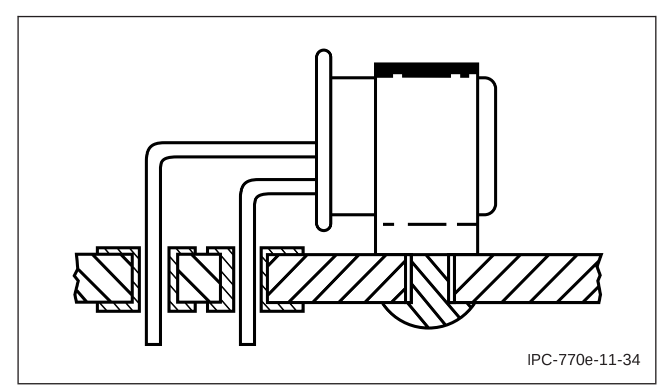


Figure 11-34 Horizontal Mounting of Radial Leaded Component

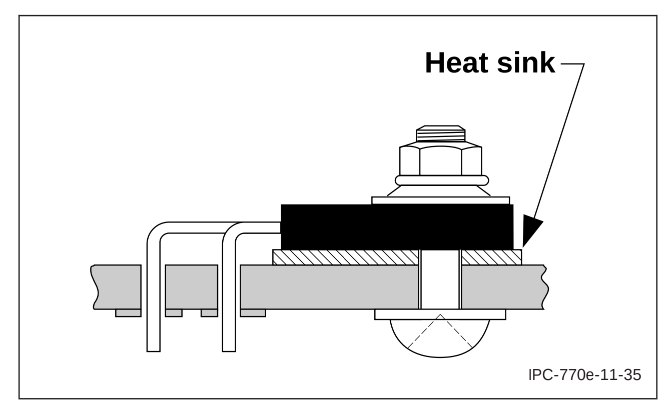


Figure 11-35 Horizontal Mounting of Radial Leaded Component with Heat Sink

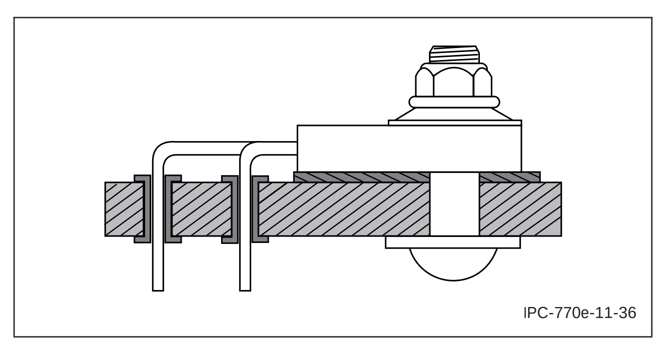


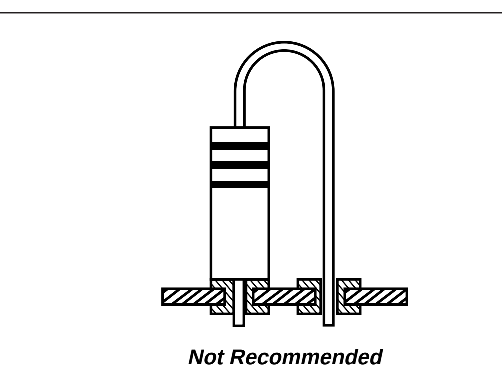
Figure 11-36 Horizontal TO Mounting

requirements should also be followed when mounting these devices.

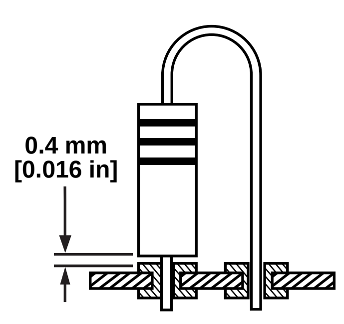
11.2.8 Electrical Insulators and Thermal Conductors When electrical insulators are also thermal conductors, the device should be in contact with the electrical insulator/thermal conductor and the electrical insulator/thermal conductor should be in contact with the board.

11.3 Vertical Mounting

11.3.1 Axial Leaded Discrete Components Components mounted perpendicular to printed wiring boards should be installed with a minimum of 0.4 mm clearance between the end of the component body, which includes any packaging meniscus and the surface of the board, to prevent potential heat damage and entrapment problems (see Figure 11-37). The maximum vertical misalignment should not violate minimum electrical spacing.



Component mounted flush to printed board.



Recommended

Component mounted with adequate clearance between end of body and board; spacer may be used.

NOTES:

1. The purpose of raising the component body off the board surface is to facilitate solder flow, escape of gases in soldering and cleaning. Normally, this is accomplished only by raising the component off the board. There are, however, certain hole devices that can support the component and still accomplish solder flow, gas liberation, and cleaning.
2. If the component is mounted tight to the board (no clearance) component movement will unduly stress the component lead.
3. Conformal coating application and coverage may necessitate an increase in the 0.015" minimum dimension.
4. Care should be taken when using spacers with high coefficients of thermal expansion.

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Figure 11-37 Vertical Mounted Axial Lead Components

11.3.2 Radial Leaded Discrete Components Components whose leads are on one side should be mounted so their axes are as parallel and perpendicular to the mounting base as practical (see Figure 11-38).

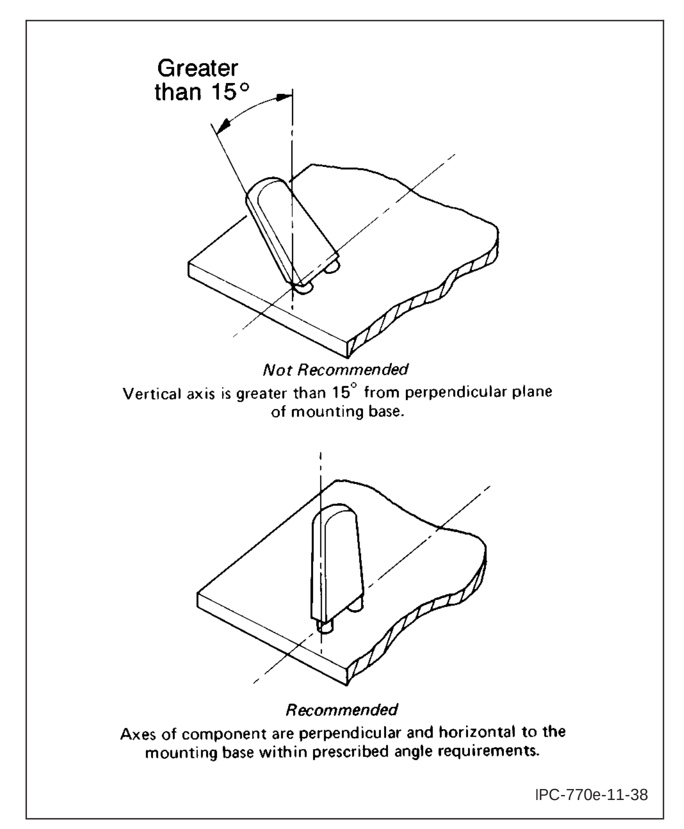


Figure 11-38 Vertical Mounted Radial-Lead Components

The coating meniscus on leads is not to be removed. Components installed on boards with lands on the component side should maintain a visible clearance between the surface of the circuitry and where the meniscus ends on the lead (see Figure 11-39). A typical method for vertical mounting in unsupported holes is shown in Figure 11-40. When required, assemblies with stringent conformal coating requirements may need some type of board coating prior to component mounting.

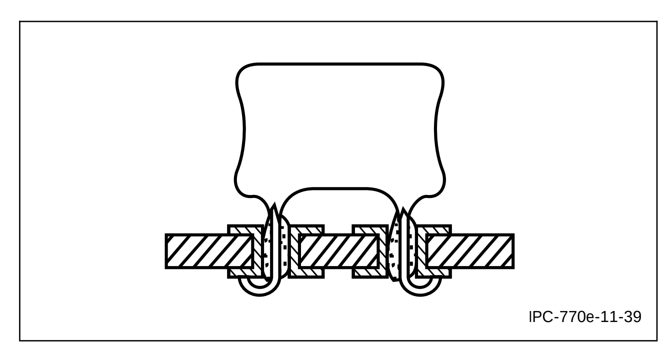


Figure 11-39 Vertical Mounted Components Coating Meniscus

11.3.3 Multiple Radial Lead Component In this method, the component leads are simply inserted in the proper reinforced hole in the printed board and joined to the land by conventional soldering techniques. A typical method for vertical mounting of a transistor without a spacer is shown in Figures 11-40 and 11-41.

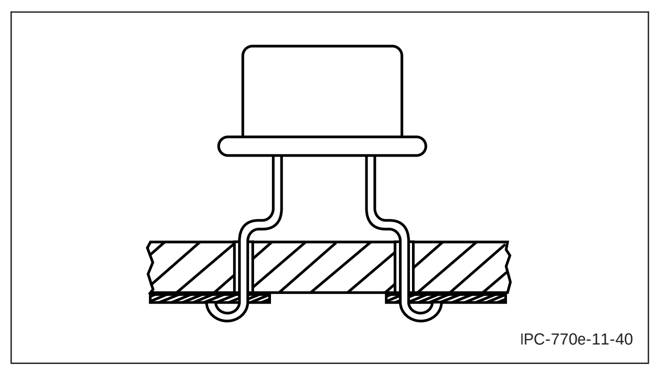


Figure 11-40 Radial Components Mounting (Unsupported Holes)

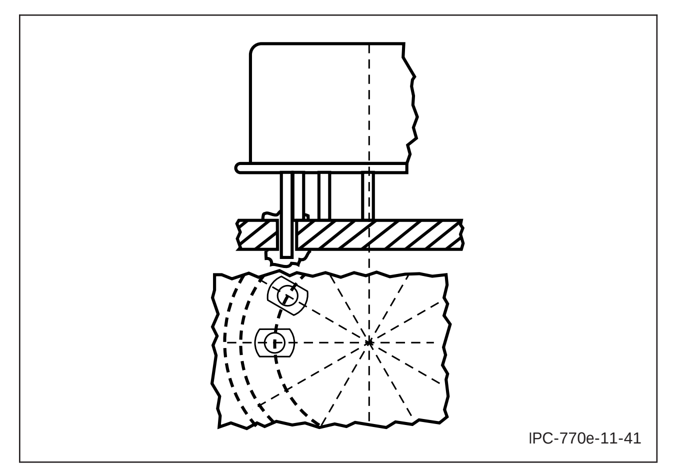


Figure 11-41 Straight-Through Lead, Unclinched Can

When used, the spacer should be installed in intimate contact to both component and printed board. Spacers with feet on one side should be mounted with the feet against the board and the component being in intimate contact with the spacer.

A typical method for mounting of a TO component with a spacer is shown in Figure 11-42. The effect of spacers on the lead/can seal and on lead forming should be evaluated before their use is determined.

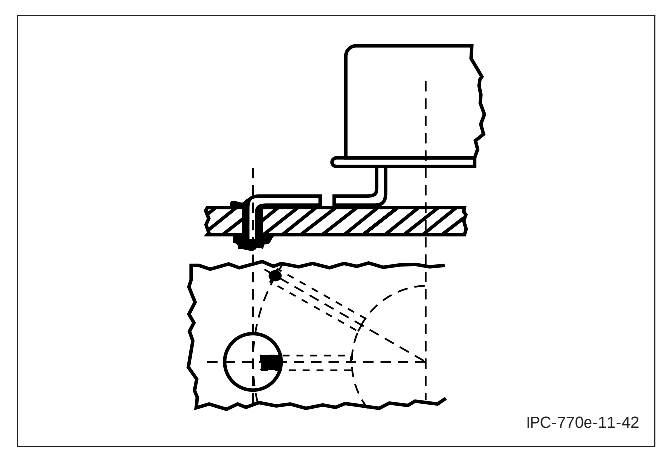


Figure 11-42 Offset Lead Can Mounting

The use of multiple lead TO can spreaders serve a similar function for offset TO can mounting as do spacers for straight-through can mounting (see Figure 11-43). Leads may be terminated in the straight-through method or the clinched lead method.

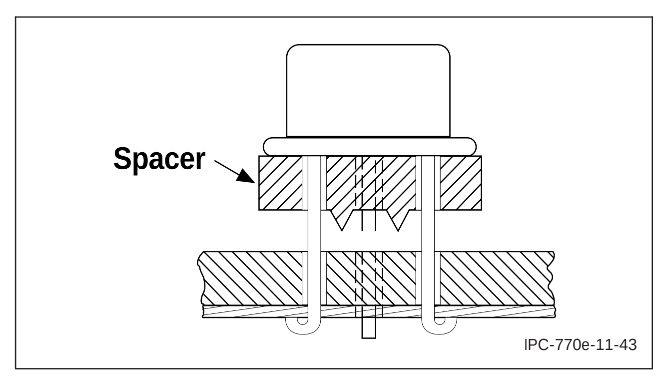


Figure 11-43 Transistor Mounting (with Spacer)

In installations where flux must be removed, a clearance should be allowed between the board and the base of the component. The base of the component should be parallel to the board.

Suitable fixturing should be provided to help assure that the component is retained in proper position throughout the soldering operation. Where no spacer is used, a temporary spacer may be required until the component has been soldered. Tab or index locations must be closely observed to assure proper orientation in mounted position.

11.3.4 Hermetically-Sealed Components Hermetically-sealed components, such as reed relays and glass-sealed capacitors and diodes, must be handled with care to prevent damage to seals.

11.3.5 Rectangular-Bodied Components A component with a rectangular body should have clearance from the mounting base to allow cleaning.

11.3.6 Metal Power Packages Metal power packages shown in Figure 11-44 should be mounted in accordance to the following:

- Lead holes may be plated through but should not be interfacial or interlayer if the component body is mounted in contact with the board or circuitry thereon.
- Component body should be spaced a minimum of 0.25 mm above the board surface if lead holes are interfacial or interlayer (to permit solder flow to and onto the component land).
- Leads may be tempered or exceed 1.25 mm in diameter provided they are not clinched against the printed board land.
- A washer should be inserted between each screw head and the land and board material (to preclude damage to the land).
- Nuts should be lock type or should be retained by locking devices.
- The heat sink or device-mounting flange may be provided with threads to match mounting screw for solder lug.
- Resilient material and/or insulating material used as required functionally or as standoffs.
- Torque specification.

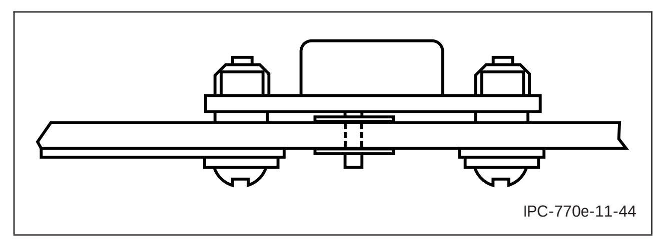


Figure 11-44 Metal Power-Package Transistor Mounted on Resilient Standoffs

11.4 Mixed Technology

11.4.1 Axial Leaded Discrete Components When through-hole axial components and chip components are used in the same assembly, care must be taken to establish proper assembly sequence, design for tool clearances and shock resistance before soldering, cleaning, inspection/testing, and rework. Refer to Section 1, general information related to Type 1 Level C or Type 2 Level C assemblies for consideration when leaded axial surface mount components are used with chip components.

11.4.2 Radial Leaded Discrete Components The assembly of surface mounted devices in combination with radial-leaded through-hole mounted devices requires two assembly processes if surface mounted devices are positioned on the same printed boards through which through-hole devices are placed.

11.4.3 Inline Leaded Components SIPs and DIPs are normally intended to be through-hole mounted. If parts are to be surface mounted the requirements on surface mounting apply. In a mixed assembly, one that contains both surface mounted and through-hole mounted components, the decision of how to mount these part types is determined during the design phase and is usually based on the number of parts of a given type with the intentions to reduce the number of assembly or process steps. Land patterns must be available for the type of attachment technique specified.

11.4.4 Pin Grid Array Components The pin grid array being through-hole mounted can be utilized along with other through-hole components, DIPs, axial-leaded components, etc., as part of a mixed assembly. Manual assembly of the pin grid array package to the printed board can be achieved by using special tools designed for ease of alignment and insertion. The operator can use a tweezer-type

device to place and hold a component, or a machine-positioned vacuum pick-up under the operator's control.

11.5 Manual Techniques See Section 1 for additional information.

11.5.1 Axial and Radial Discrete Components Procedures to be employed follow practices to reduce contamination and damage to the components. Identification marking is desirable on printed wiring to assure proper placement of components during assembly.

11.5.2 Dual-Inline Package Gripping Tools Tools may be used to maintain lead spacing during insertion (see Figure 11-45).

11.5.3 Multiple Radial Leaded Discrete Components Special tools and equipment are not normally needed or used for manual insertion of multilead radial components.

11.5.4 Inline Leaded Components Special fixtures or forming techniques may be required to maintain component placement/position integrity prior to the solder process. As an alternative, partial assembly and soldering may be required before a second set of electronic components are mounted to the packaging/interconnection structure.

11.6 Automated Techniques Refer to Section 8 for general considerations. Some basic principles for assembly, especially automated, are:

- Arrange all components on X and, if necessary, Y axes.
- Arrange components in columns and/or rows, if possible.
- Sequence all types of axial lead components prior to insertion.
- Minimize the distance between the components and follow a grid pattern for component layout.
- Minimize the number of different center spacings.
- Make provisions for tooling holes at or near the edge of the board in an area not occupied by components.
- Minimize the number of different hole sizes to minimize manufacturing time if boards are drilled or die costs if punched.
- Provide clearance areas, as large as the tooling footprint between components, for the insertion tools both above and below the board.

11.6.1 Axial Leaded Discrete Components Multiple station sequencers and automatic variable center distance (VCD) axial component insertion machines can be utilized to perform high labor content kitting and component preparation automatically for manual or operator-assisted



Figure 11-45 Dual-Inline Package Gripping Tools

component assembly. For this application, the cut and clinch head of the VCD machine is removed and a multiple cavity tray is placed in a modified board holder in place of a printed board.

11.6.2 Radial Leaded Discrete Components Attention should be given to control insertion forces on preformed leads so as to not compromise clearance of components from printed board surface to assure sufficient clearance for cleaning after assembly.

11.6.3 Multiple Radial Lead Components When the radial method of automatic insertion of the TO-5, TO-18, and similar families of devices is used, the leads must generally be prepped prior to the insertion operation, i.e., straightened and cut.

There are few standards for automatic insertion of TO can type components because very few are inserted automatically. There are two general methods for automatic insertion of transistors: axial when the leads handle the part and radial when the body handles the part.

A factor to be considered with the radial insertion is the uncertainty of lead position caused by the fact that leads cannot be guided directly into the board holes. Generally, the component hole diameter must be increased at least an additional 0.25 mm to allow for lead position variation.

11.6.3.1 Location Considerations Both axial and radial insertion require tooling clearances. Above-the-board clearances similar to those in Figure 11-46 must be used in the axial method. The radial method requires a clearance around the body diameter of approximately 2.0 mm larger than the body.

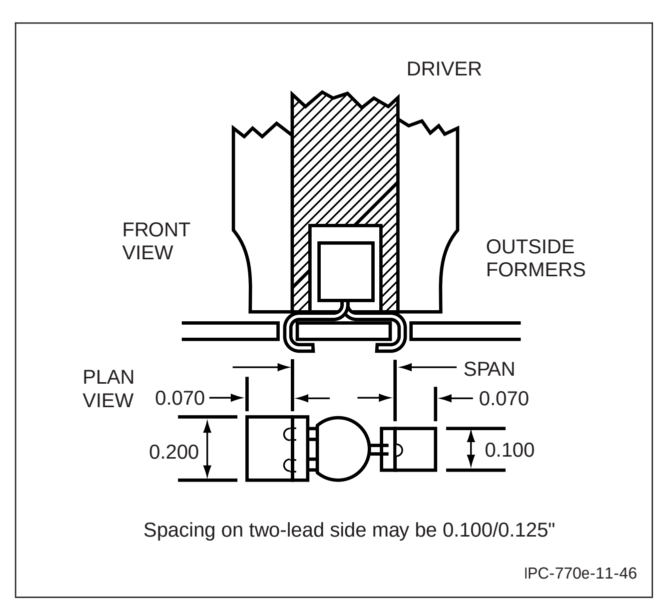
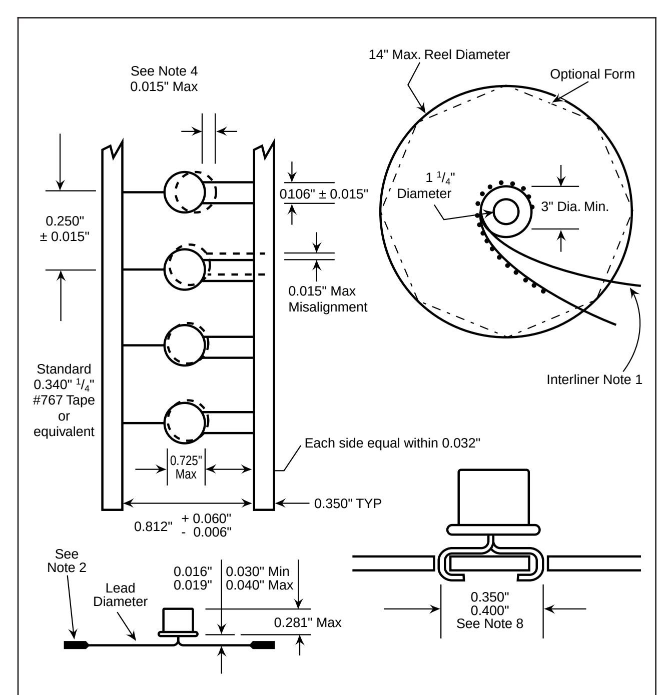


Figure 11-46 Transistor Assembly Tools

11.6.3.2 Radial Method The component body is held during the insertion process for means of inserting and locating the part on the board. After the leads are prepped, the major problem with the radial technique is that the physical configuration of the parts varies substantially from batch to batch, and from manufacturer to manufacturer.

11.6.3.3 Axial Method When the axial method of automatic insertion is used, the transistor is treated like an axial-leaded component. This system for handling TO-92, TO-18, and similar transistors is based on forming the leads as shown in Figure 11-47 and taping them on conventional lead tape, just like an axial-leaded component.



Notes:

1. Heavy Kraft or single ply "A" type corrugated interliner to be used.
2. Lead length in contact with tape, each side, 0.120" minimum.
3. Leads must be straight within 0.015" between body and tape.
4. Component bodies must be in line within 0.015".
5. No more than one component may be missing at a gap.
6. Distance between tapes must not go below minimum shown. Variation of 0.060" over reel permissible.
7. Both in-line leads (TO-92, TO-98, etc.) and TO-18 pin configurations suitable for this process.
8. Insertion spacing is a function of part width. For example: for 0.235" width, it is 0.400". Certain plastic devices can be handled down to 0.300".

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Figure 11-47 Taping Specifications (only inches shown)

Since the physical configuration of the component can vary due to manufacturers' processes, it is advisable to obtain parts on reels with thick interliners. This would ensure the handling of one-size part only.

Once on tape, the insertion problem becomes one of compatible wire diameter since only the leads and a body clearance to a maximum envelope handle the part. As a result,

a single insertion head without retooling can use nearly all vendors' devices. Spans from 7.6 to 10.2 mm are possible.

11.6.4 Inline Leaded Components Dual-Inline-package (DIP) integrated circuits are among the most common electronic devices to be processed. The obvious advantages of automatically inserting DIPs are speed, volume, and accuracy. In nearly all cases of printed board design where DIPs are used, it is recommended that all DIPs be inserted in a single orientation.

The component space requirements for DIP components are similar to axial lead components in that the general rules for axial lead component layout apply whenever they are intermixed with DIPs on the same board. The DIP to DIP clearances for the tooling fingers are shown in Figure 11-48. In all cases of board design because the front leads locate the DIP, it is recommended that all DIPs be laid out in a row or column fashion, starting at the front or ''operator'' side of the board (see Figure 11-49).

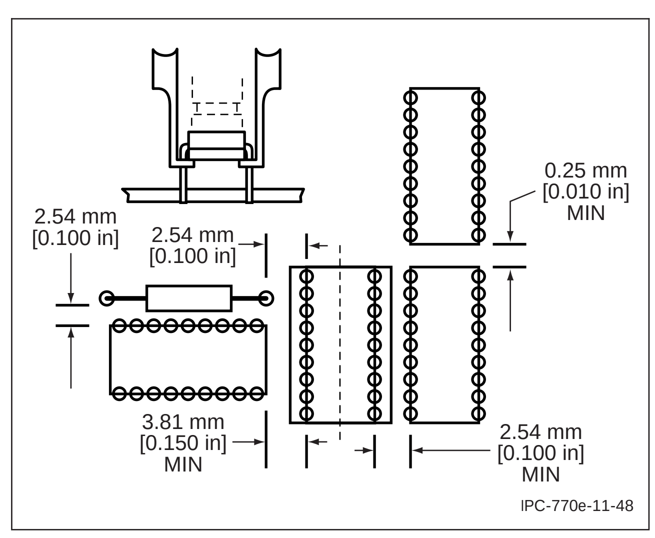


Figure 11-48 DIP Clearances

The DIP leads should be uniform and not bent too far from the specified positions. Machines do form and straighten the leads within the machine, but leads bent too far out of tolerance cannot be formed and will cause jams in the machine. Care should be taken not to damage lead to body seals on ceramic metal devices.

For automatic insertion, the DIP components should be obtained from the supplier in slide magazines. See Figure 11-50 for feeding into the insertion machines. Each slide magazine can hold from 20 to 50 DIP components. The capacity of the slide magazine depends upon the length of the DIP.

DIP components may be inserted into sockets mounted on the printed boards as well as directly into predrilled holes. Wherever it is desired to insert into sockets rather than directly into the circuit board, the cut and clinch mechanism can be disabled. In the case of wire wrap sockets, the

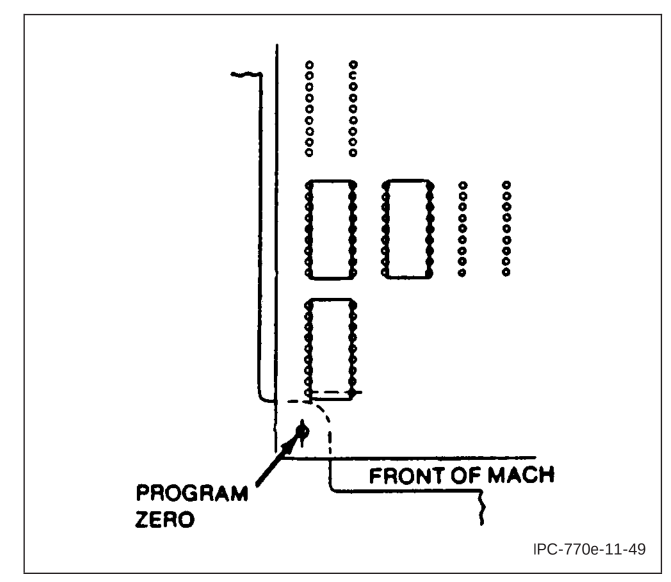


Figure 11-49 DIP Layout in Rows and Columns

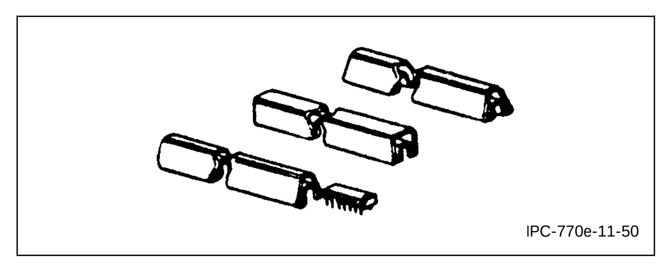


Figure 11-50 DIP Slide Magazines

cut and clinch mechanism may be completely removed to provide the necessary clearance for the socket leads. Sockets are not acceptable on Class 3 products.

Pin Grid Array Components – For high volume pin grid array package assembly, high accuracy assembly robot work cells represent a cost effective method of automating semiautomatic and manual steps. The work cells can be configured to perform a wide variety of insertion and assembly tasks.

12 COMPONENT CHARACTERISTICS SURFACE MOUNT

12.1 Characterization and Classes

12.1.1 Part Type Descriptions

12.1.1.1 The 1.27 mm [0.0500 in] Center Family Figure 12-1 shows six variations of the package center family. The four leadless types, Type A, B, C and D provide different orientations depending on the type, the mounting structure, and the preferred thermal orientation. The leadless packages are typically ceramic packages with hermetically sealed metal or ceramic lids. Leadless types E and F are also defined for low I/O devices.

The 1.27-package center family, which includes both leadless and leaded devices, is designed to mount on a common mounting pattern. This package family is transitional in

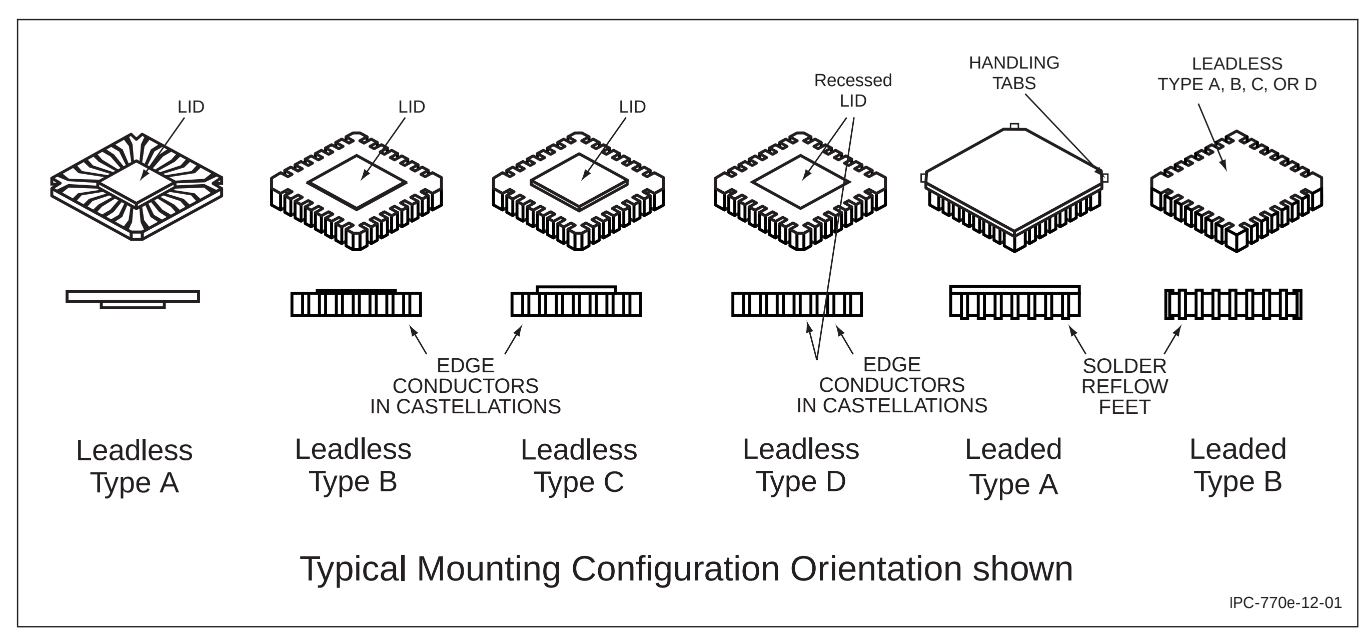


Figure 12-1 50-mil Center JEDEC Packages

that some packages are hard metric while older designs use imperial units (inches). Designers are cautioned not to mix devices or package types without consideration of this fact. They can be directly attached to the mounting structure or can be plugged into sockets. Figure 12-2 shows some of the common features of the 0.0500 inch family. One basic restriction is that there should be no terminals in the corners of the package. There are a number of common sizes in the 1.27 mm center family; they include 20-, 28-, 44-, 52-, 68-, 84-, 100-, 124- and 156-input/output terminal sizes. The leadless type C also includes 16-, 20- and 24-terminal package.

12.1.1.2 Leadless Chip Carriers A leadless chip carrier is a ceramic or plastic package with integral surface-metallized terminations. Leadless types A, B and D chip carriers have a chamfered index corner that is larger than that of type C. Another difference is that types A, B and D are designed for socket applications and printed wiring interconnections. Type C is primarily intended for direct attachment through reflow soldering. This difference in application is the main reason for their mechanical differences. All have compatible terminal locations. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation (see Figure 12-2).

Leadless type A is intended for lid-down mounting in a socket, which places the primary heat-dissipating surface away from the mounting surface for more effective cooling in air cooled system. Leadless type B is for lid-up socket mounting on printed board or for direct soldering to other types of substrates. Type C is a ceramic package similar to leadless type B except for corner configuration and type D is for lid-down mounting on a substrate (see Figure 12-2).

12.1.1.3 Leaded Chip Carriers The leaded type A chip carrier is either a ceramic or plastic package with compliant leads and can be socketed or soldered to substrates. Leaded type B chip carriers are leadless packages with clip leads. They are handled similarly to the leaded type A, but leaded type B chip carriers should be soldered to the substrate since the leads are not suitable for socketing (see Figure 12-3).

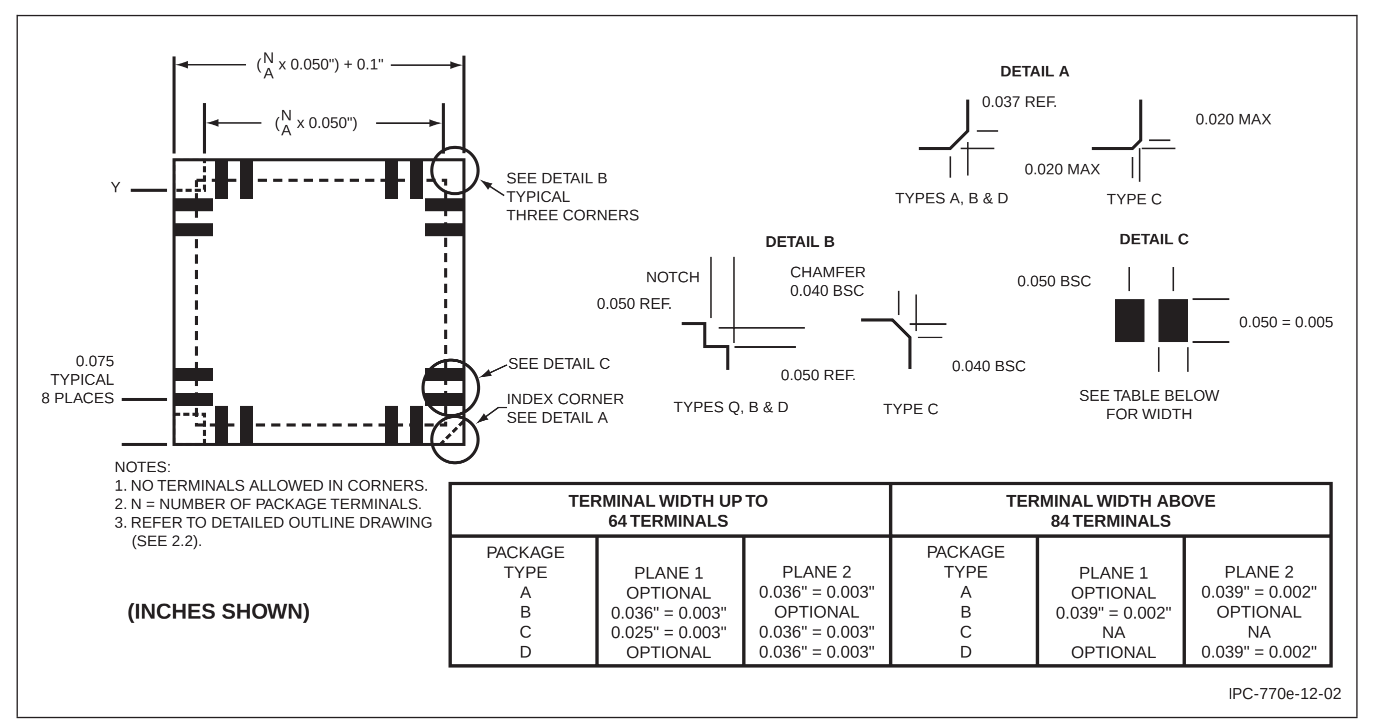
A leaded package is considered one of the following:

- A chip carrier with integral surface mount compliant leads. This is typified by the JEDEC leaded type A package (MS006 and MS007) having leads formed along the side and under the package body, allowing for socket insertion or for solder attachment directly to the substrate.
- A leadless chip carrier having surface-mount or through-hole clip leads. The JEDEC leaded type B package (MS008) is typical of this type.

12.1.1.4 The 1.02 mm Center Family The 1.02 mm family is of ceramic leadless construction and originally intended for direct attachment to ceramic substrates. The family includes chip carriers with 16-, 20-, 24-, 32-, 40-, 48-, 64-, 84- and 96-input/output terminals.

In addition, JEDEC recently proposed a rectangular variation of this package with 32 I/O and staggered terminals.

12.1.1.5 The 0.635 mm Center and 0.50 mm Center Families The JEDEC 1.27 mm and 1.02 mm centerline standard chip carriers are inefficient for 100 to 124 terminal counts. To solve some limitations of JEDEC chip carriers for packaging LSI and VLSI circuits with high terminal counts, an ad hoc task group was established through the IEEE Computer Society's Technical Committee on



TERMINAL WIDTH UP TO 64 TERMINALS			TERMINAL WIDTH ABOVE 84 TERMINALS		
PACKAGE TYPE	PLANE 1	PLANE 2	PACKAGE TYPE	PLANE 1	PLANE 2
A	OPTIONAL	0.036" = 0.003"	A	OPTIONAL	0.039" = 0.002"
B	0.036" = 0.003"	OPTIONAL	B	0.039" = 0.002"	OPTIONAL
C	0.025" = 0.003"	0.036" = 0.003"	C	NA	NA
D	OPTIONAL	0.036" = 0.003"	D	OPTIONAL	0.039" = 0.002"

Figure 12-2 Features Common to 0.050 inch Center Packages

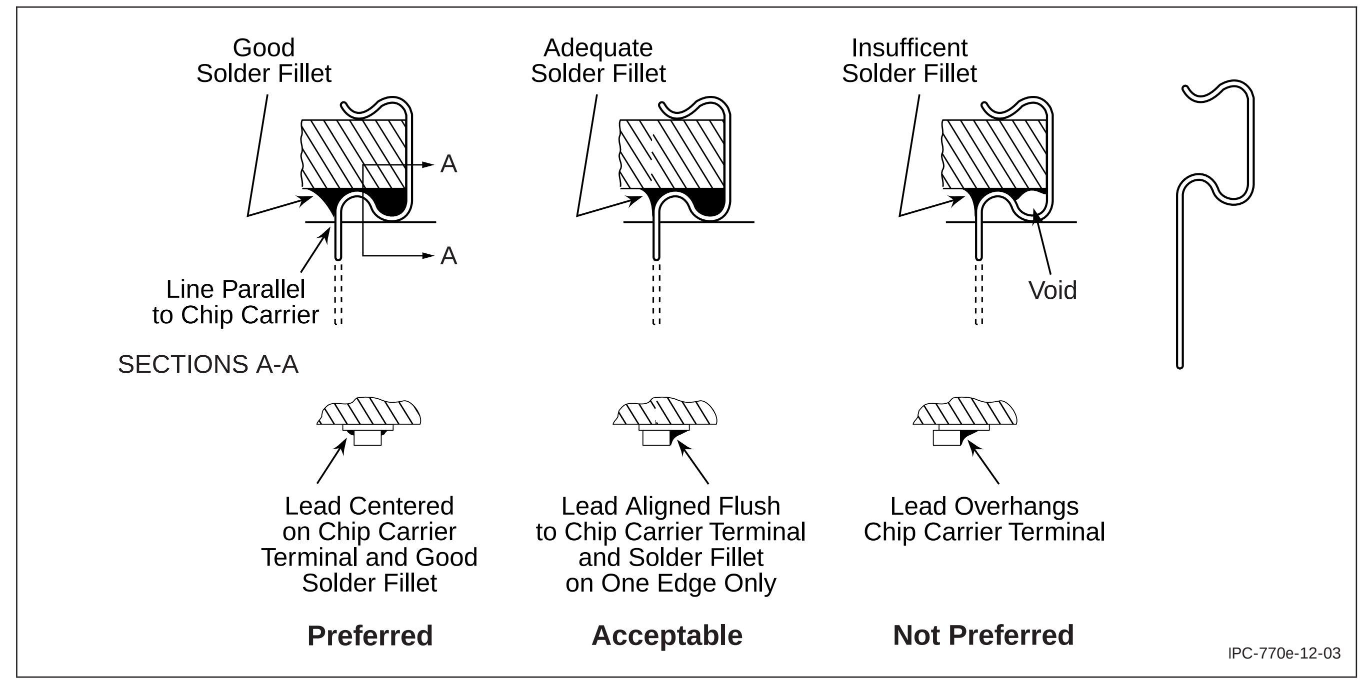


Figure 12-3 Criteria for Lead Attachment to Leadless Type A to Make a Leaded Type B

Packaging in late 1980. The group agreed on a number of basic requirements:

- Both 0.5 and 0.635 mm centerline spacing chip carrier packages should be used and standardized.
- Ceramic and plastic packages should be standardized following the compatible-mounting concept of the JEDEC 1.27 mm standard packages.
- Certain mechanical tolerances must be maintained and specific mechanical features for socketing are required.
- All sizes would specify corner notches; no chamfers are recommended except in the index corner.
- Reference notch to terminal centerline tolerance should be 0.05 mm.
- Land width for the 0.635 mm spacing should be 0.3 mm, and for the 0.5 mm spacing, 0.25 mm.
- If possible, use ceramic sizes common to JEDEC standard packages.

A set of outline drawings has been accepted by JEDEC for this fine pitch family. Lead counts and ceramic sizes are shown in Table 12-1.

Table 12-1 JEDEC Ceramic Sizes and Fine Pitch Terminal Count

JEDEC Ceramic Size	Terminal Count	
	0.635 mm	0.50 mm
0.450	52	64
0.560	68	N/A
0.650	84	104
0.750	100	124
0.950	132	164
1.150	164	204
1.350	196	244
1.450	N/A	264
1.550	N/A	284
1.650	244	304

12.1.1.6 Double-Row Plastic Chip Carrier This surface mounting plastic chip carrier nearly doubles the number of available pins in standard sized units. For example, the design for the 0.150 cm^2 size, occupied by a 68-pin standard plastic leadless chip carrier provides 128 pins in two rows of surface mount leads around the carrier's perimeter (see Figure 12-4).

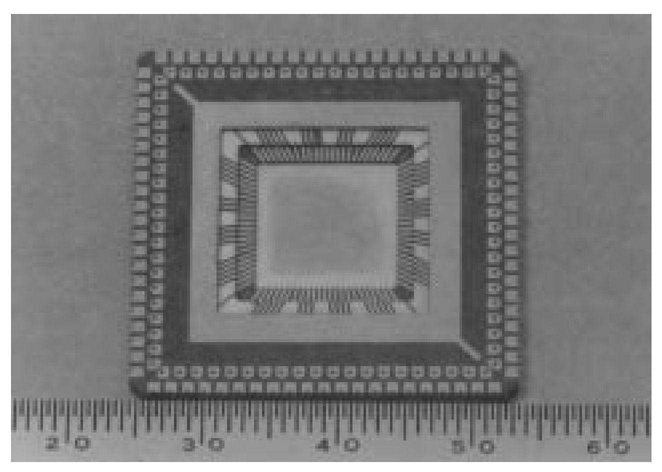


Figure 12-4 Double Row Plastic Chip Carrier

After indentation, the leads in the individual rows are still separated by standard 1.27 mm spacing. A castellated structure holds the two rows of pins an inner and an outer row 1.27 mm apart. Within each row the leads are on 1.27 mm centers. In the new two-row design, the wiring traces to the outer row proceed along the outside of the carrier. However, the traces to the inner row pass through the board and proceed on the board's underside to other points in the board circuit. This way, the spacing and width of the traces to a double-row chip carrier remain standard.

12.1.1.7 Glass Epoxy Leadless Chip Carriers A glass epoxy chip carrier consists of three parts: a metallized base, a cavity wall and a lid to enclose the package. The base is a double-sided plated-through-hole glass epoxy printed board (normally FR-4, although other materials can be used) containing a number of outlines in array formats. The cavity walls are formed by routing out holes in another piece of glass epoxy board that is then press laminated to the base. The array is then sliced into individual chip carriers with a standard diamond impregnated dicing saw. The lids are made in similar arrays and also sliced up with the dicing saw.

The photographic precision of the metallization together with the accuracy of the dicing saw operation yield an extremely clean package with very close dimensional tolerances and smooth edges with no fiber dust in the bonding area. The smooth edges and surfaces together with the close tolerances make these packages particularly adaptable to automatic assembly, testing and handling equipment.

The conductors are made from clad copper laminate that is electroplated 5 microns thick with copper, then nickel 0.125 to 0.250 micron thick and finally gold 0.05 micron to 0.1 micron thick. This combination of metallization provides an excellent base for automatic wire bonding in the cavity area, and yet does not put enough gold on the footprint to embrittle the solder joint.

12.1.1.8 Package Materials and Construction Chip carriers are available in many constructions and materials comparable to Dual-Inline packages (DIPs).

Plastic premolded chip carriers, recommended primarily for commercial application, have the advantages and drawbacks of a plastic DIP: low cost, not hermetically sealed, 0°C to 70°C operating temperature range and nominal environment protection. Some of these packages are rated at -25°C to 85°C operating temperature.

Glass-frit sealed chip carriers are similar in construction to ceramic DIPs (Cerdips). They are hermetic and are environmentally testable, costing more than the plastic construction but less than the solder-sealed carrier. They are candidates for some high-reliability packaging applications, but some require special handling to avoid damage to the package. Solder-sealed 3-layer chip carriers are equivalent of solder-sealed DIPs. These hermetic devices are the most expensive chip carriers because of high gold content. However, seal temperature is lower than that of the lower cost Cerdip-type.

12.1.1.9 Plastic Package Chip Carrier There are two types of plastic chip carriers: premolded and postmolded. Both types are composite metal/dielectric assemblies that include a conductor lead frame and a molded insulating body. The premolded chip carrier has one or more apertures for mounting microelectronic elements, while the

postmolded chip carrier is a complete assembly without apertures. The package manufacturer performs all necessary plating operations to eliminate plating or tinning by the user.

12.1.1.10 Ceramic Package Chip Carrier The ceramic chip carrier is usually constructed from a 90° to 96° alumina or beryllia base, using a single layer or multilayer co-fired metallization process originally developed for the DIP. The metallization is generally a trimetal combination of a refractory metal (such as tungsten or molybdenum), nickel and gold.

12.1.1.11 Type Designations The 1.27 mm center and 1.02 mm center chip carrier standard families have the JEDEC designations and can be found in JEDEC 95-83.

12.1.1.12 Component Considerations Direct soldered leadless ceramic chip carriers exhibit lower junction to board thermal resistance as compared to leaded chip carriers. However, the rigid interface is more susceptible to solder joint cracking due to thermal expansion mismatch between the component packages and the substrate.

The compliant leads of the leaded packages are designed to absorb thermally induced stress. Copper alloy leads with thermal and electrical conductivity higher than those used for DIPs are used in some leaded plastic chip carriers to facilitate lead forming and thermal coupling to the substrate.

Component packages with the cavity up (i.e., with the heat-radiating surface adjacent to the substrate) are typically chosen for military systems in which a substrate is cooled by conduction to the assembly structure.

12.2 Component Procurement

12.2.1 Packaging Almost every kind of multiterminal device is available in chip component form. The most common are chip resistors, chip capacitors and diodes, but linear magnetic devices (chokes and transformers), crystals, and even more complex devices, are made in chip form. Refer to IPC-D-279 for DfR recommendations.

12.2.1.1 Part Description Chip component sizes range from chip diodes on the order of 0.6 mm x 0.6 mm to large capacitors that are over 9.0 mm x 2.5 mm. Most other chip components can be solder assembled to printed board structures with assembly technologies similar to those described for through-hole mounted components.

The most common package shape for resistors, capacitors and many other types of component is the rectangular chip. It is rectangular in profile and in cross section and it has metallized terminations on each end. Figure 12-5 shows a typical rectangular chip resistor and Figure 12-6 shows several common configurations of rectangular capacitors. Electronic Industries Association standard RS-198 covers ceramic dielectric chip capacitors and RS-228 covers fixed electrolytic tantalum chip capacitors.

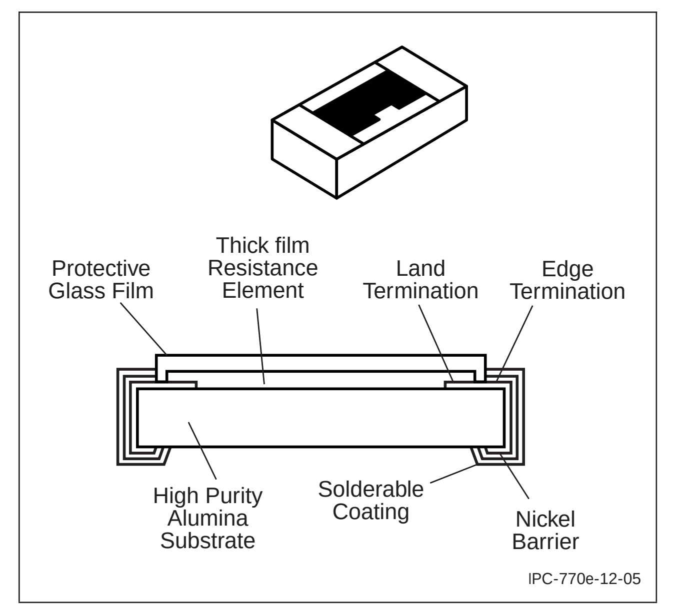


Figure 12-5 Common Configurations of Rectangular Resistors

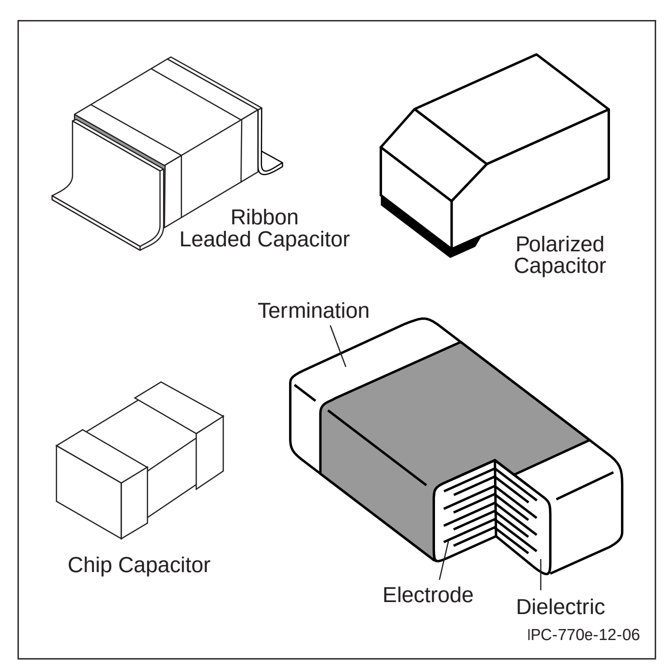


Figure 12-6 Typical Rectangular Chip Capacitors

Some components, especially diodes and high power resistors, are available in tubular or cylindrical metal electrode face form (commonly called MELF). Other devices have the terminations arrayed on the bottom of the device rather than on the ends or can have pads located on the top surface of the component for wire bonding to lands on the mounting substrate. Special care is required to assemble most of these custom components.

The end terminations typically have a solder plate or solder dip finish but some have gold, palladium or silver-palladium finish. For solder assembly tin or tin alloy, finish is preferred with a copper or nickel barrier to prevent any silver of the internal contact from leaching. The end terminations can exhibit any of the configurations shown in Figure 12-7. The ''five-faced'' termination is preferred. Single-faced terminations exhibit significantly poorer assembly yields than either the three- or five-faced configurations.

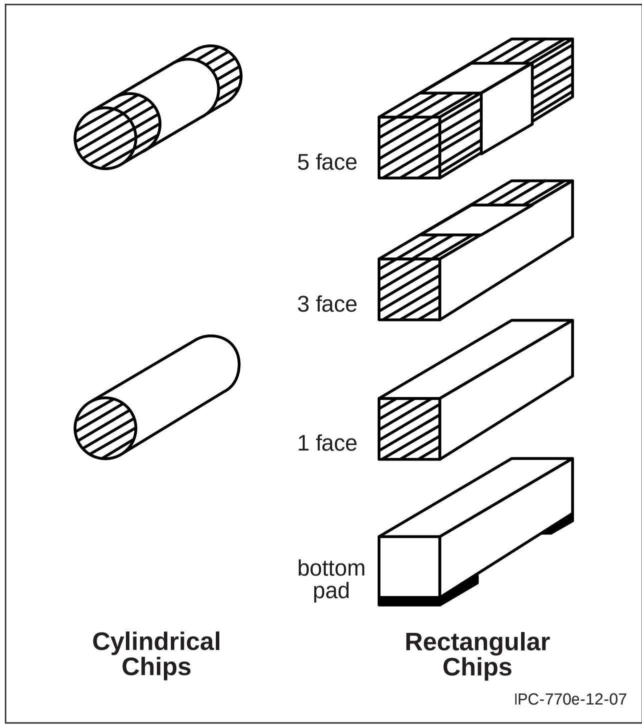


Figure 12-7 Cylindrical/Rectangular Terminations

12.2.1.2 Chip Inductors Chip inductors are available in either ceramic or ferrite variations. Typical wire used is polyurethane/nylon insulated copper magnet wire, ranging in size from 38 AWG to 48 AWG. The terminations are usually molybdenum, manganese or nickel coated with 95% tin, 5% silver solder. Typical outlines are shown in Figures 12-8 and 12-9.

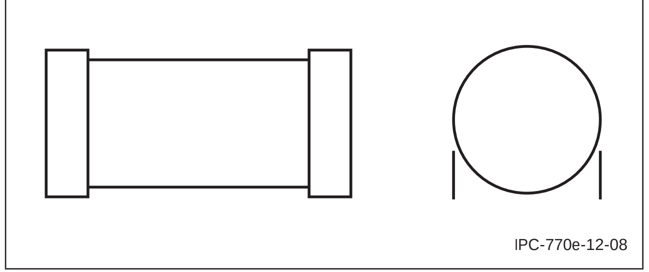


Figure 12-8 A Chip Inductor

12.2.1.3 Switches Switches in surface mount configurations are now becoming available. DIP, slide, push button, rotary DIP and toggle switches are available which withstand the temperatures of batch or mass soldering as well

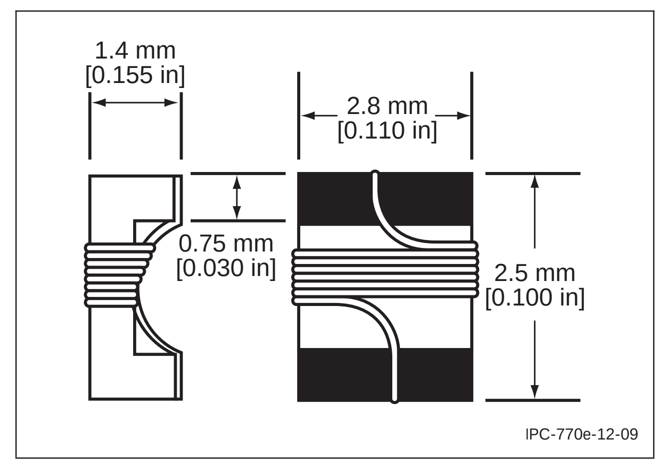


Figure 12-9 Typical Surface Mount Inductor

as immersion cleaning. SMD switches usually have ''I'' lead, ''J'' lead or ''L'' lead. To ensure solder connection reliability, the lead configuration must provide for thermal expansions while providing a mechanically sound solder joint during switch actuation.

12.2.1.4 Other Devices Other passive devices are being adapted to surface mounting applications. One noteworthy example is a surface mount sealed single-turn cermet trimmer in a vertical and horizontal style. This particular product is available in a 1K to 200K ohms resistance range. Figure 12-10 shows an outline of this trimmer.

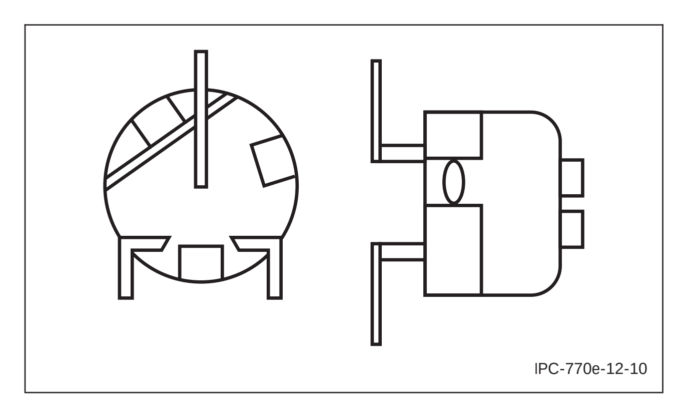


Figure 12-10 Surface Mount Cermet Trimmer

12.2.1.5 Small Outline Component Small outline (SO) components are available in a series of molded plastic packages with 0.0635 mm [0.025 in] pitch and up to 0.127 mm [0.050 in] pitch. They are designed for surface mounting to the printed board or to other substrates; and therefore, are supplied in gull wing or J-leaded configuration. SO package outlines are included in JEDEC 95-83.

12.2.1.5.1 SOIC Packages Small outline integrated circuit (SOIC) packages can have eight, fourteen, sixteen, twenty, twenty-four, twenty-eight leads or more and fall into two groups. The leads are arrayed as two rows of leads with adjacent leads spaced 1.25 mm apart. In the smaller component group, consisting of SO-8, SO-14, and SO-16

packages, the rows are spaced about 6.0 mm apart. In the group of larger components, consisting of SO-16L, SO-20, SO-24 and SO-28 packages, the rows of leads are about 10.0 mm apart. A typical SOIC package is illustrated in Figure 12-11.

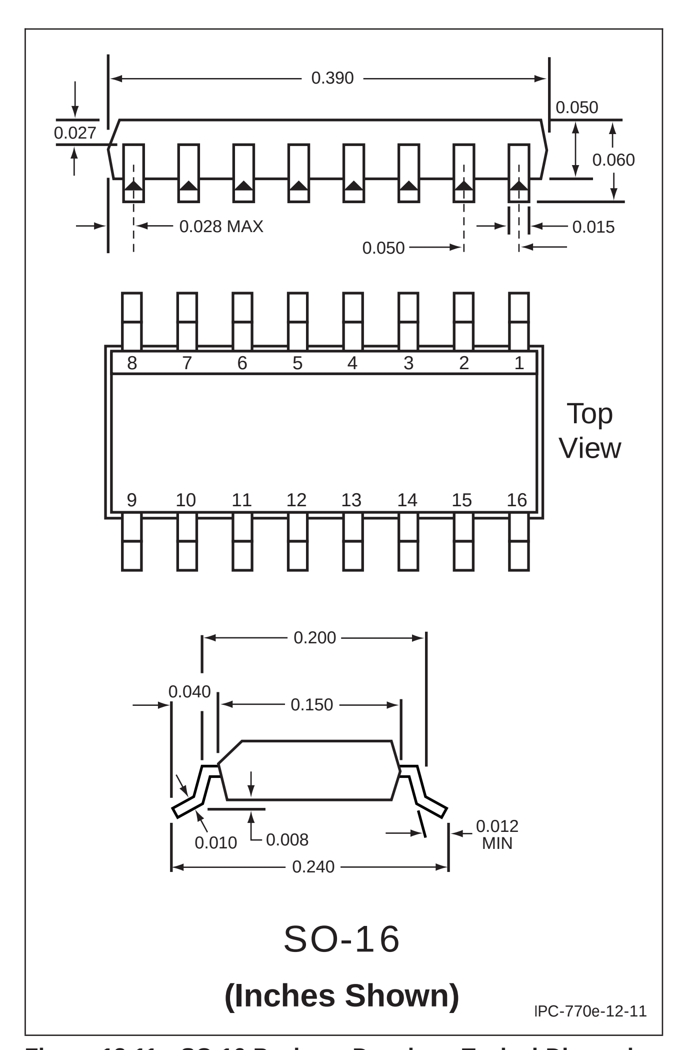


Figure 12-11 SO-16 Package Drawings Typical Dimension

12.2.1.5.2 SOT Packages Three leaded components are designated SOT packages. Two common SOT packages are the SOT-23 and SOT-89. In general, SOT packages are used with diodes, transistors and small I/O devices (devices with only a limited number of input-output lead requirements). SOT packages are illustrated in Figure 12-12.

Chip carriers can be generally defined as low profile, square packages with connections on all four sides consisting of metallized terminations on ‘‘leadless’’ version and on the ‘‘leaded’’ type the leads are attached to the sides of the package and formed into gull wing or J-leaded configurations.

Some disadvantages in the component mounting process are inherent to the use of either leaded or leadless chip carriers. These include the need for more precise placement techniques and the requirement for retaining the component in place prior to the soldering operation. Other general considerations are outlined in Table 12-2.

The use of leaded chip carriers generally has the following advantages over leadless chip carriers:

- The effect of thermal expansion mismatch is less critical with leaded chip carriers due to lead compliance.
- Flexure of a substrate structure is less critical with leaded chip carriers due to lead compliance.
- Leaded chip carriers can be more readily used with the glass/polymer (epoxy, polyimide or bismaleimide triazine) printed boards and do not generally require ceramic substrates or constrained core boards. Printed boards made with random aramid fibers have a lower coefficient of thermal expansion and are often used with leaded carriers that must withstand higher operating temperatures or higher range in operating environment temperatures.
- The leads create a standoff that aids in the removal of soldering fluxes during cleaning.

The use of leaded chip carriers generally has the following disadvantages when compared to the use of leadless chip carriers:

- When used, the application of clip leads requires additional process and inspection steps, thereby increasing costs.
- The length of leaded chip carrier terminals can significantly increase lead inductance.
- The leaded chip carrier package does not have as direct a path to conduction cooling through the substrate.
- Leads can be damaged in test and assembly.
- Planarity of leads must be maintained for reliable solder joints.

12.2.2 Delivery System

12.3 Handling and Storage The handling and storage of chip components should be in accordance with the guidelines in 3.4.

12.3.1 ESD Protection Refer to 3.4.1.2.

12.3.2 Moisture Plastic bodied components are susceptible to absorption and retention of moisture. Component manufacturers categorize components to a moisture sensitivity level with IPC/JEDEC J-STD-020A. This level of sensitivity determines the methods of preservation required to assure that the components do not crack or delaminate (popcorn) in the manufacturing process. IPC/JEDEC J-STD-035 provides a test method for determining if damage has occurred during the manufacturing process. IPC-9501, 9502, 9503 and 9504 provide guidance on conditioning of components prior to assembly. IPC/JEDEC J-STD-033 provides detailed instructions for handling and storage of moisture sensitive devices.

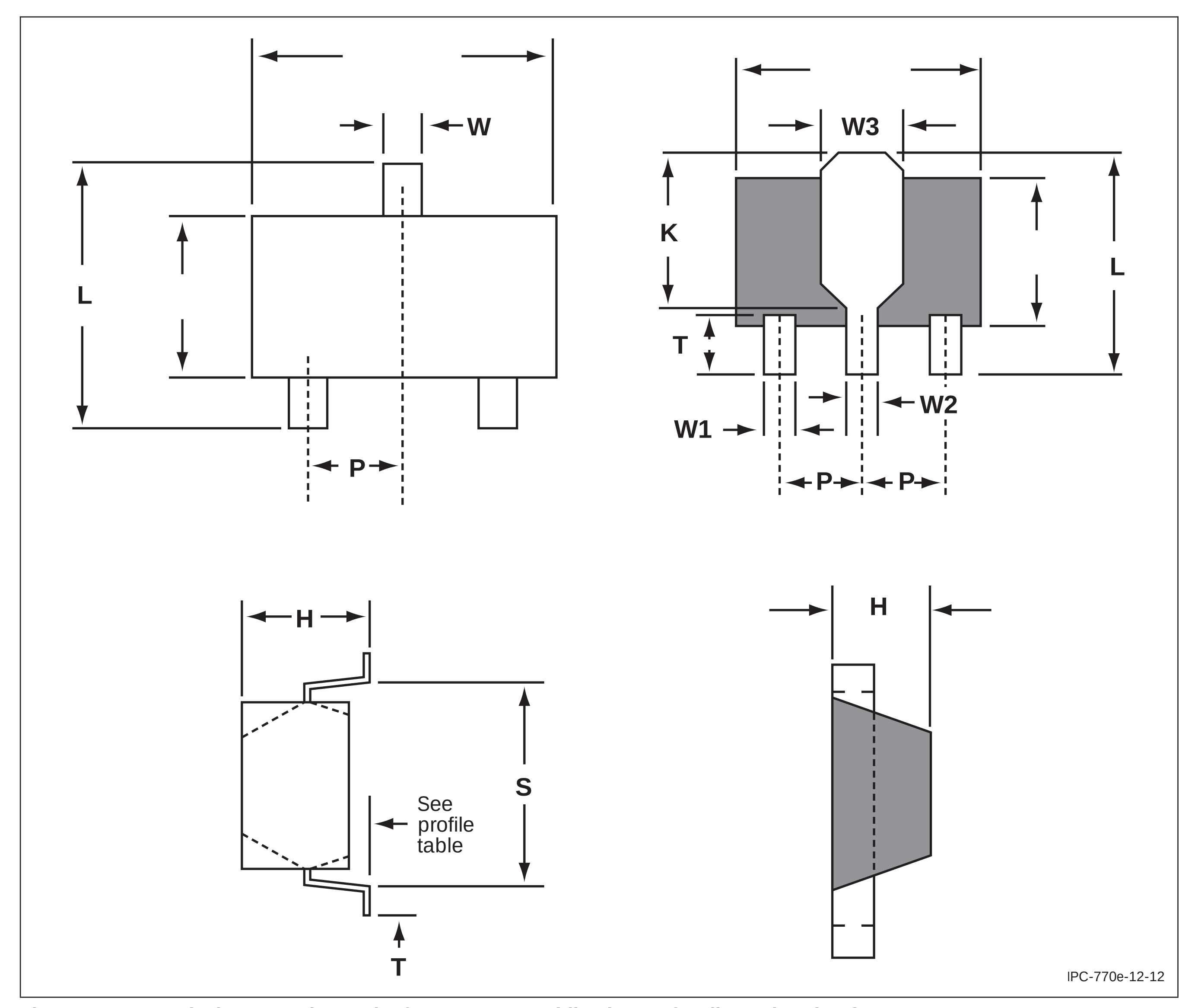


Figure 12-12 Typical SOT Packages (Refer to JEDEC Publication 95 for dimension data.)

Printed circuit boards are also susceptible to moisture absorption and can exhibit deterioration of solderability as a result of that moisture during the assembly process. Because of the complexity and variables associated with boards, the user needs to determine the specific storage or baking time and temperature requirements.

12.4 Chip Resistors

12.4.1 Basic Construction The resistive material is applied to a ceramic substrate and terminated symmetrically at both ends with a ‘‘wrap around’’ metal U-shaped band. The resistive material is face-up, thus trimming to close tolerances is possible. Since most equipment uses a vacuum-type pickup head, it is important that the surface of the resistor is made flat after trimming. Otherwise, the vacuum pickup might be difficult (see Figure 12-13).

12.4.2 Termination Materials End terminations are solderable. Solder can be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. A tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

12.4.3 Marking Resistors equal to or larger than 2012 mm [0805 in.] are labeled. Resistors smaller than 1608 mm [0603 in] are generally unlabeled.

12.5 Chip Capacitors

12.5.1 Basic Construction Multilayer ceramic capacitors use substrate materials such as alumina for hybrid circuits and porcelainized metal. The monolithic construction used in producing these chips results in a solid block of ceramic with an enclosed electrode system and metallized ends for circuit attachment. This solid block is rugged and capable of withstanding the harsh environment and treatment associated with manufacturing processes (see Figure 12-14).

Table 12-2 General Application Considerations

Consideration	Leadless CCs	Leaded CCs
Thermal expansion to match	Critical	Moderate
Removal and replacement	Comparatively easy with special tools	Less risk of damaging packaging and interconnecting structure
Solder joint inspection	Difficult	Moderate
Flux removal after solder	Difficult	Moderate
Socket compatible	Yes (except Type C)	Yes (except Type B)
Lead length	Minimal	Moderate (inductance greater)
Conductive cooling	Good, with direct lead conduction path (lower profile height)	Poor (higher profile height)
Preparation for soldering	Solder coating of terminals required	None except for solder coating as required for solderability
Self centering	Usually	Rarely
Flexure of substrate	Critical	Moderately

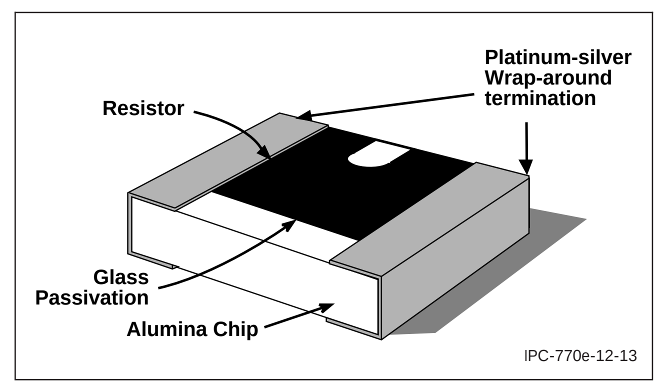


Figure 12-13 Basic Chip Resistor Construction

Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consecutive drying and firing eliminates the organic components and effects a bond between the ceramic dielectric and glass constituent in the termination.

12.5.2 Termination Materials End terminations are solderable. Solder can be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. A tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination is symmetrical and does not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination covers the ends of the components and extends out to the top and bottom of the component.

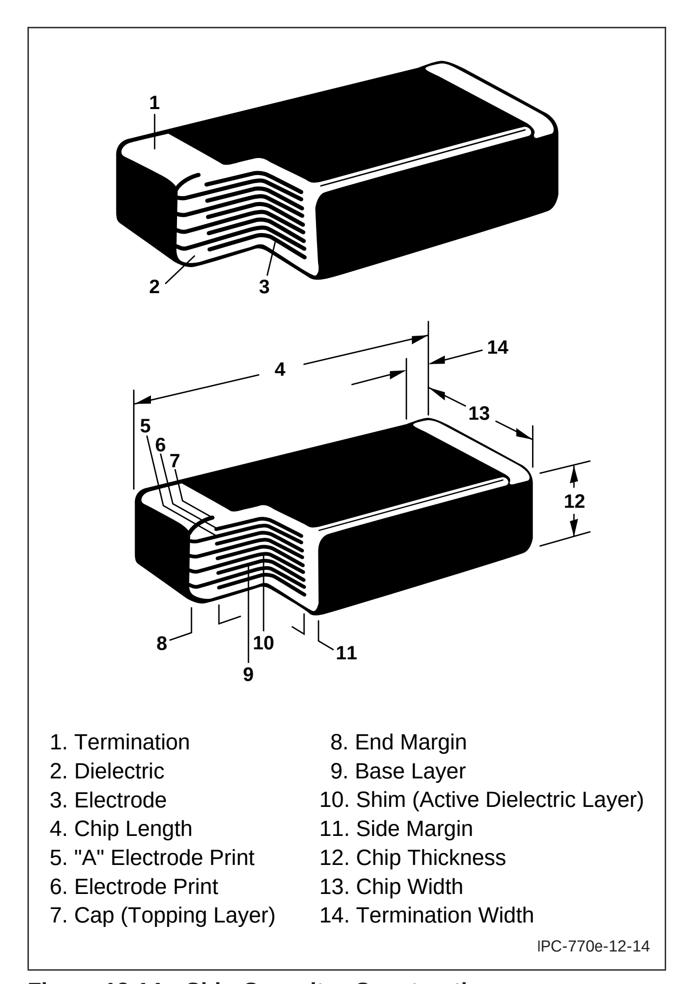


Figure 12-14 Chip Capacitor Construction

Most common termination materials include palladium-silver alloy, silver and gold. Solder finish applied over precious metal electrodes has a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier and should be at least 0.00125 mm [0.00005 in] thick.

12.5.3 Marking Ceramic capacitors are typically unmarked.

12.6 Inductors

12.6.1 Basic Construction At the time of publication, there was no industry standard document for leadless inductors. The dimensions were taken from manufacturer's catalogs, but only when at least two component vendors manufacture the same package. However, the same inductor value cannot be available in the same package from the two manufacturers (see Figure 12-15).

12.6.2 Termination Materials End terminations are solderable. Solder can be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation

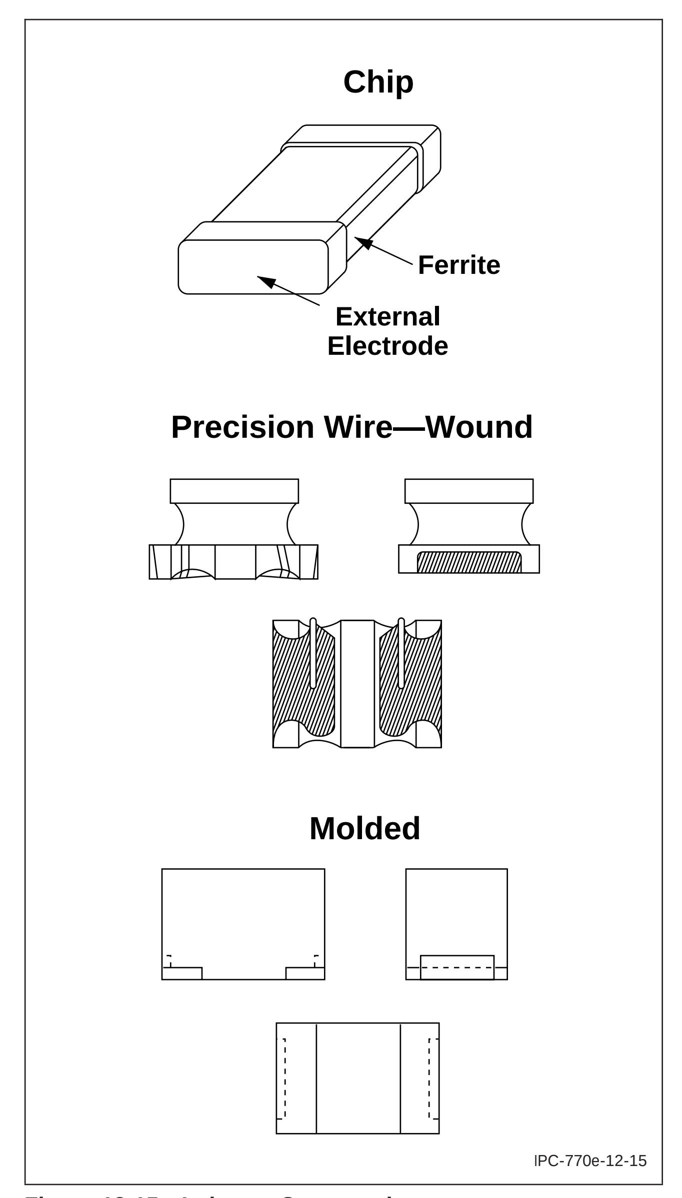


Figure 12-15 Inductor Construction

to fuse the solder. A tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination is symmetrical, and does not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and extends out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes will have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

12.6.3 Marking Parts are available with or without marked inductance values.

12.7 Tantalum Capacitors A variety of values exist for tantalum capacitors. The following sections describe the most common types.

12.7.1 Basic Construction See Figure 12-16.

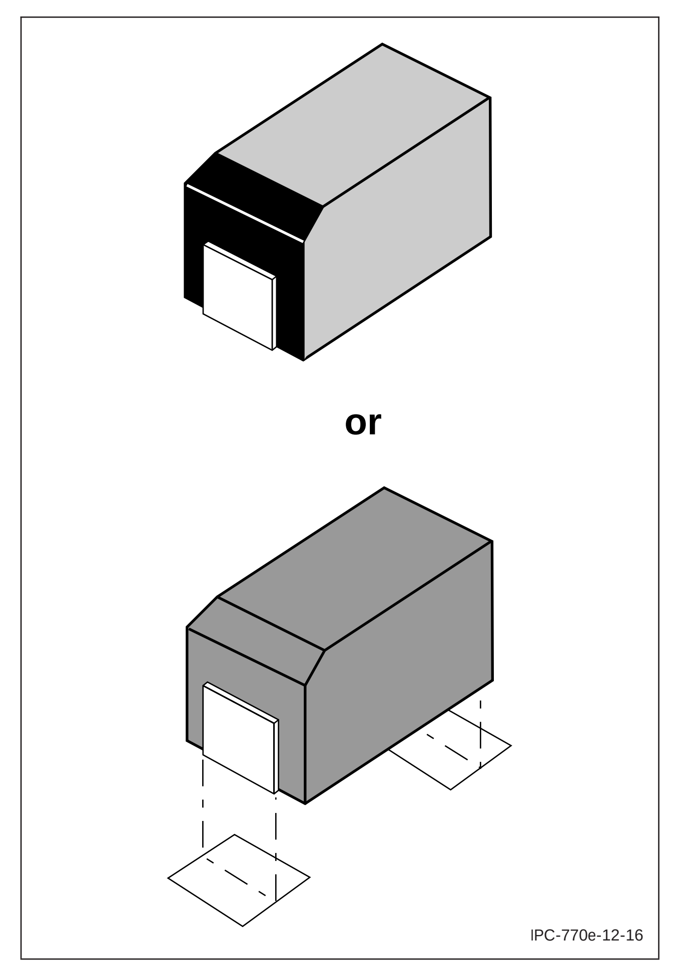


Figure 12-16 Tantalum Capacitor Construction

12.7.2 Termination Materials End terminations are solder-coated with a tin/lead alloy. Solder can be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. A tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

12.7.3 Marking Parts are available with or without marked capacitance values.

12.8 Metal Electrode Face (MELF) Components Resistors, diodes, ceramic capacitors, and tantalum capacitors can all be packaged in these tubular shapes.

12.8.1 Basic Construction Figures 12-17a and 12-17b.

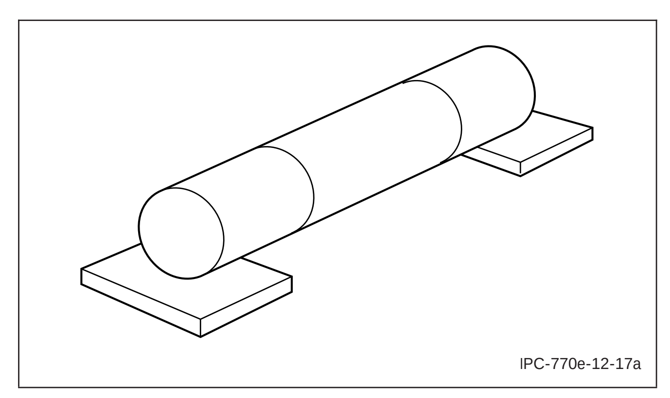


Figure 12-17a Metal Electrode Face Component

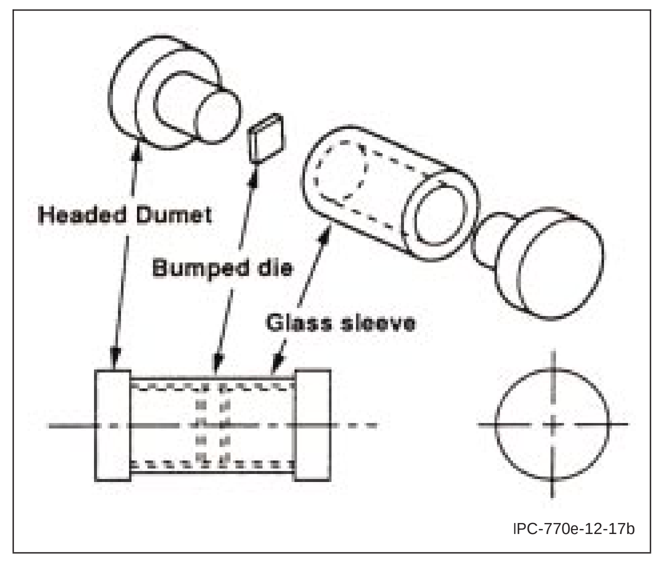


Figure 12-17b Break-Away Diagram of MELF Components Construction Figure

12.8.2 Termination Materials End terminations are solderable. Solder can be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. A tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The terminations should be symmetrical, and should not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination covers the ends of the components, and extends around the entire periphery.

The most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

12.8.3 Marking Parts are available with or without marked values.

12.9 SOT 23 One of the first active devices in packaged form for surface mounting was the SOT device. Plastic encapsulated three terminal devices with leads formed out from the body were surface mounted to overcome some of the problems and difficulties in handling dip transistors. In general, SOT packages are used with diodes, transistors, and small I/O devices.

The SOT 23 package is the most common three-lead surface mount configuration.

12.9.1 Basic Construction The SOT 23 package has had several redesigns to meet the needs of both hybrid and printed board surface mount industries. These changes resulted in low, medium and high profile characteristics that basically reflect the clearance that the body is from the mounting surface (see Figure 12-18).

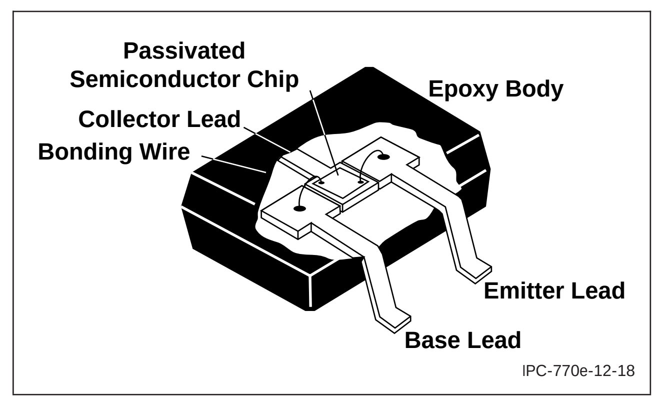


Figure 12-18 SOT 23 Construction

12.9.2 Termination Materials Leads are a solderable finish.

12.9.3 Marking Parts are available with or without marked values.

12.10 SOT 89 These parts are for high power transistors and diodes. These parts are used where heat transfer to a supporting structure is important.

12.10.1 Basic Construction The SOT 89 package dimensions are designed to meet the needs of both the hybrid and printed board surface mount industries. In order to provide an adequate heat transfer path, there is no clearance between the body of the component and the packaging and interconnect structure. This design can accommodate the reflow or wave soldering processes (see Figure 12-19).

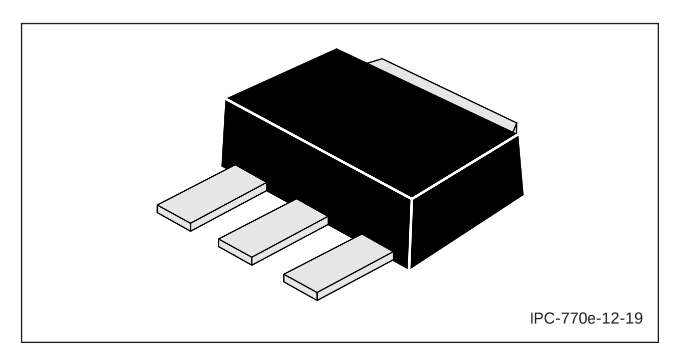


Figure 12-19 SOT 89 Construction

12.10.2 Termination Materials Leads must have a solderable finish.

12.10.3 Marking Parts are available with or without marked values.

12.11 SOD 123

12.11.1 Basic Construction The small outline diode comes in two configurations, gull wing-leaded and molded with terminations. The gullwing-leaded configuration is shown in Figure 12-20.

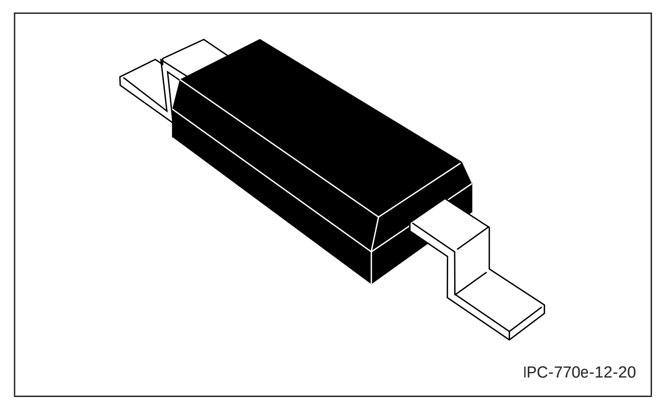


Figure 12-20 SOD 123 Construction

12.11.2 Termination Materials Leads are a solderable finish.

12.11.3 Marking Parts are available with or without marked values.

12.12 SOT 143 These parts are for dual diodes and Darlington transistors.

12.12.1 Basic Construction The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.05 to 0.13 mm [0.002 to 0.005 in] to accommodate reflow or wave soldering processes (see Figure 12-21).

12.12.2 Termination Materials Leads must have solderable finish.

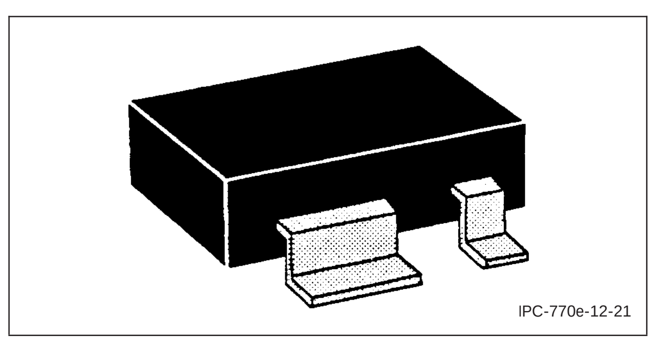


Figure 12-21 SOT 143 Construction

12.12.3 Marking Parts are available with or without marked values.

12.13 SOT 223 These parts are for dual diodes and Darlington transistors.

12.13.1 Basic Construction The dimensional characteristics are designed to meet the needs of the surface-mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.06 mm (basic) to accommodate reflow or wave soldering processes (see Figure 12-22).

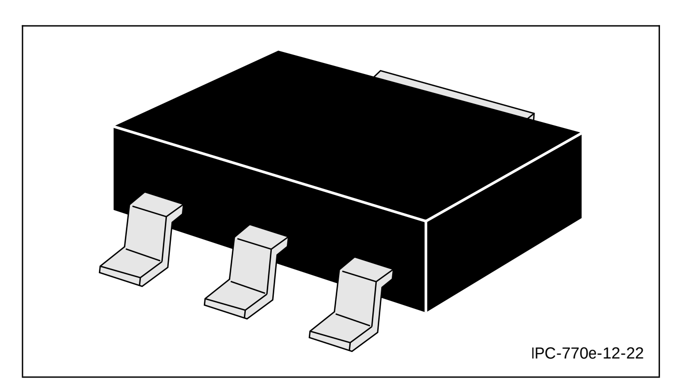


Figure 12-22 SOT 223 Construction

12.13.2 Termination Materials Leads must have solderable finish.

12.13.3 Marking Parts are available with or without marked values.

12.14 TO 252/TO 268 These parts are for dual diodes and Darlington transistors.

12.14.1 Basic Construction See Figure 12-23.

12.14.2 Termination Materials Leads must have a solderable finish.

12.14.3 Marking Parts are available with or without marked values.

12.15 SOIC These components are all on 1.27 mm pitch, and are available in narrow (3.90 mm), wide body (7.50 mm) and extra wide body (8.90 mm) sizes, ranging from 8 to 36 pins.

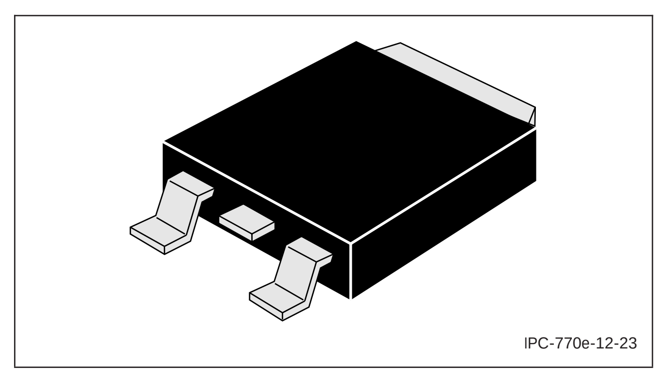


Figure 12-23 TO 252 Construction

12.15.1 Basic Construction See Figure 12-24. Basic construction consists of a plastic body and metallic leads.

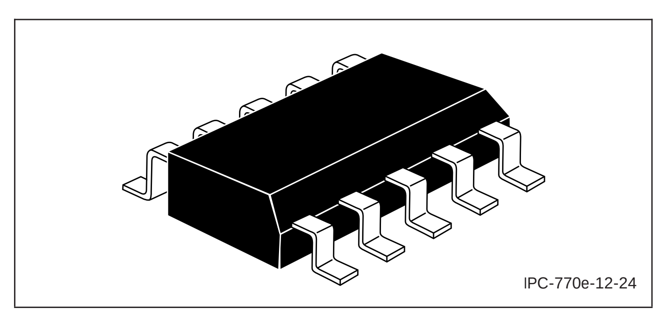


Figure 12-24 SOIC Construction

12.15.2 Termination Materials Leads must have a solderable finish.

12.15.3 Pin Numbering All parts are marked with a part number and pin 1 location. The pin 1 location can be molded into the plastic body.

12.16 SOP

12.16.1 Basic Construction IPC-SM-782 has defined center-to-center spacing for the land pattern slightly differently than is indicated in the EIAJ specification ED 7402-1.

This specification allows for six families of the SOP. EIAJ classifies the families by the center-to-center distance of the land patterns and the outer extremities of the leads (dimension ''L'' in IPC-SM-782). The basic construction of the SOP specified by EIAJ is the same construction as for SOIC specified by JEDEC. Both have gull wing leads on 1.27 mm centers.

The EIAJ specification allows for a number of positions of the components to be in any of the families (e.g., body width). The sizes shown in Figure 4-25 are the most common, however, there are Type II SOP 14s and there are also Type I SOP 16s (see Figure 12-25).

12.16.2 Termination Materials Leads must have a solderable finish.

12.16.3 Marking Parts are available with or without part number markings. Usually an index mark indicates pin 1.

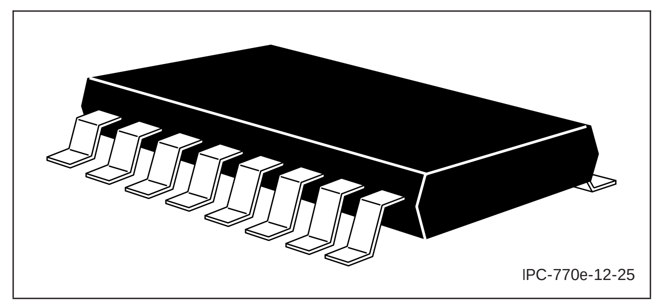


Figure 12-25 SOPIC Construction

12.17 SOJ The two-sided J lead family is a small outline family identified by the dimension of the body size in inches. For example, the SOJ/300 has a body size of 0.300 inches or 7.63 mm, the SOJ/350 has a body size of 0.350 inches or 8.88 mm, the SOJ/400 has a body size of 0.400 inches or 10.12 mm, and the SOJ/450 has a body size of 0.450 inches or 11.38 mm. Package lead counts typically range from 14 to 28 pins.

The small-outline ''J'' (SOJ) package has leads on two sides, similar to a DIP. The lead configuration, like the letter J, extends out the side of the package and bends under the package forming a J bend. The point of contact of the lead to the land pattern is at the apex of the J bend and is the basis for the span of the land pattern.

The leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, no lead can be more than 0.1 mm off the flat surface.

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory ICs are often used in multiples, and buss lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of ''J'' leads. With high capacity memory systems, the space savings can be significant.

12.17.1 Basic Construction

12.17.2 Termination Materials Leads must be solderable finish.

12.17.3 Marking The SOIC family of parts is generally marked with manufacturers part numbers, manufacturers name or symbol, and a pin 1 indicator. Some parts can have a pin 1 feature in the case shape instead of a pin 1 marking. Additional markings can include date code/manufacturing lot and/or manufacturing location.

12.18 PLCC (Square) Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C to 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages (see Figure 12-26).

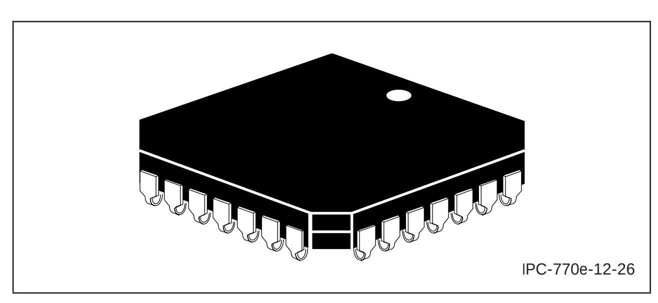


Figure 12-26 PLCC (Square)

12.18.1 Premolded Plastic Chip Carriers The premolded plastic chip carrier was designed to be connected to the packaging and interconnecting substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement and allow for substrate warpage as high as 0.5%. Solder attach to the packaging and interconnecting substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

12.18.2 Post-Molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the premolded package that has an aperture for mounting microelectronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, the package manufacturer to eliminate tinning or plating performs all necessary plating operations by the user.

The Joint Electronic Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, 124, or more leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages, which have J-lead configuration and are JEDEC standard MO-047, are available in 20, 28, 44, 52, 68, 84, 100, 124 or more lead counts with the same spacing.

12.18.3 Marking All parts shall be marked with a part number and pin 1 location. The pin 1 location can be molded into the plastic body.

12.19 PLCC (Rectangular) Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C to 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages (see Figure 12-27).



Figure 12-27 PLCC (Rectangular) Construction

12.19.1 Premolded Plastic Chip Carriers The premolded plastic chip carrier was designed to be connected to the packaging and interconnecting structure by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the packaging and interconnecting structure is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

12.19.2 Post-Molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the premolded package, which has an aperture for mounting microelectronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, the package manufacturer to eliminate tinning or plating performs all necessary plating operations by the user.

The Joint Electron Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, 124 or more leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

12.19.3 Marking All parts are marked with a part number and pin 1 location. The pin 1 location can be molded into the plastic body.

12.20 LCC

12.20.1 Basic Construction A leadless chip carrier is a ceramic package with integral surface-metallized terminations. Leadless Types A, B, and D chip carriers have a chamfered index corner that is larger than that of Type C. Another difference between the A, B, and D types and Type C is the feature in the other three corners. The types A, B, and D, were designed for socket applications and printed wiring interconnections. The Type C is primarily intended for direct attachment through reflow soldering. Type C is a ceramic package similar to leadless Type B except for corner configuration. The 50 mil center family, which includes both leadless and leaded devices, is designed to mount on a common mounting pattern. This application difference is the main reason for their mechanical differences. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation.

Leadless Type A is intended for lid-down mounting in a socket, which places the primary heat-dissipating surface away from the mounting surface for more effective cooling in air-cooled systems.

12.20.2 Termination Materials Leads must be solderable finish.

12.20.3 Marking All parts will be marked with a part number and pin 1 location. The pin location can be molded into the plastic body.

13 MOUNTING STRUCTURE GUIDELINES SURFACE MOUNT

13.1 Printed Board Characterization and Types The details for printed board characterization and types are defined in Section 1, Table 1-1.

13.2 Organic Rigid, Organic Flex and Rigid-Flex The details for organic rigid, organic flex and rigid-flex are defined in Section 1.

13.3 Land Patterns Land patterns must be designed for maximum assembly yield. Land sizes must be large enough to ensure an adequate fillet at the extremes of allowable board and component tolerances while not wasting space needed for routing and other component mounting. Appropriate land and mounting patterns for the individual components are contained in the respective sections for the components considered. Surface mount land patterns are addressed in IPC-SM-782.

Land patterns for mounting chip components should be designed for high assembly yield in order to maintain product performance and high reliability of the finished product. Various land shapes are used to solder attach chip components, the most common being rectangular, circular or diamond shaped lands. Some variants such as ovals, semicircles or rectangles with rounded corners are also used. Figure 13-1 shows some typical land configurations (see IPC-SM-782 for more details).

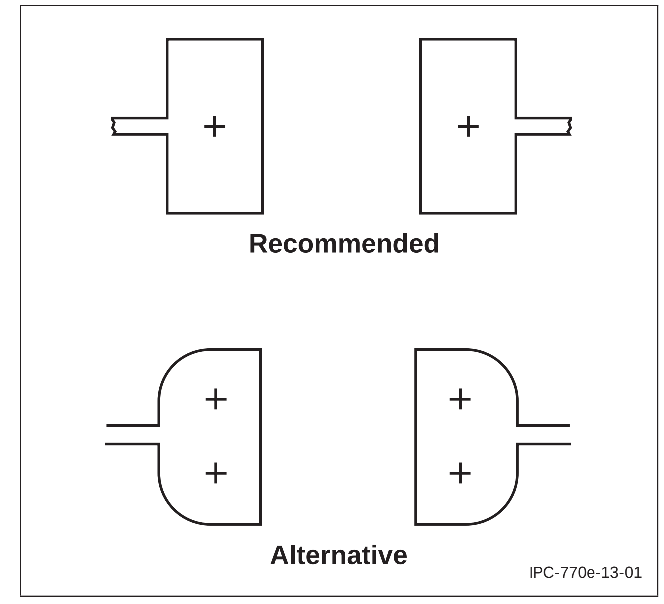


Figure 13-1 Chip Component and Lands

Printed Wiring Board (PWB) lands for the solder assembly of rectangular chip components should be approximately the same width as the component terminations. Lands that are significantly narrower than the component do not provide adequate space for the formation of good fillets and lands that are much wider than the part waste space. Lands that are either too narrow or too wide can allow too much lateral motion of the part.

If the components are attached to the substrate with adhesive before soldering the size and shape of the land is less critical than when the components are held in place with solder paste and reflowed. Very wide or very narrow lands are undesirable for solder paste reflow assembly because they allow excessive motion of the component during the reflow process. Lands for cylindrical (MELF) components should have a width approximately equal to the diameter of the component. Adhesive bonding of cylindrical parts to the substrate is recommended for both wave and reflow soldering.

The length of the bonding land for rectangular chips must be adequate to provide a satisfactory fillet at the allowable extremes of the tolerances for board, placement and component dimensions. For components that are bonded to the substrate for wave soldering, the primary limitations on the length of the land are the requirements of the solder process. Either the length of the land must be restricted or other measures must be taken to prevent excessive solder

build-up on the end terminations of the components. Excess solder on the end terminations can damage the components.

When parts are held to the lands with solder paste and then reflow soldered, the lands must also be restricted to limit the motion of the part during reflow soldering to prevent ‘‘tombstoning.’’ Tombstoning occurs when chip components fail to make a joint at one end and rotates and stands on the other end of the land.

The spacing between the inner edges of the lands should be approximately the distance between the inner edges of the terminations on the components. If the distance between lands is greater than the distance between the component termination, the solder at the joint can be inadequate and if the spacing between the lands is significantly less the parts can move excessively during soldering.

The outside corners of lands on wave soldered assemblies are commonly rounded or cut off to reduce the incidence of solder bridges to adjacent board features. Cutting or rounding the corners on the inside of the land pattern does not reduce bridging and can impair the solder fillet formation for parts that are displaced toward the land edge and should not be done.

13.4 Tolerance Analysis The following tolerance concepts are used to determine the land patterns for electronic components. These concepts are detailed in Table 13-1 and reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Table 13-1 Tolerance Analysis Elements for Chip Devices

Tolerance Element	Detailed Description
Component tolerance	The difference between the MMC and the LMC of each component dimension, length, width and distance between electrodes or leads. This number is the ‘‘C’’ tolerance in the equations.
Board tolerance	The difference between the MMC and the LMC of each land pattern dimension. This number is the ‘‘F’’ tolerance in the equations.
Positional accuracy	Placement accuracy defined as Diameter of True Position, DTP. This is the variation of the part centroid related to the land pattern theoretical centre. 0.1 - 0.2 mm DTP.
Toe fillet	0 04. - 0.6 mm
Heel fillet	Land protrusion beyond the internal lead or termination dimensions. 0.0 - 0.2 mm
Side fillet width	Land protrusion to either side of the lead or termination. -0.02 - 0.02 mm

Solder joint minima are shown for toe, heel and side fillets. These conditions are minimal, since the land pattern equations in IPC-SM-782 address the tolerance of component, board, and placement accuracy tolerances (sum of the squares). The minimum solder joint or land protrusion is increased by the amount that the tolerance variation does not use up.

The courtyard excess is added to the maximum dimension that the land pattern or component occupies. The excess number is added to each side of the dimension in question. This addition is intended to provide sufficient room for electrical and physical clearance between components and/or land patterns. Since the total of all the number calculation cannot result in a clean numerical equivalent a suggested round-off feature has been added to the tables to identify a rounded-up final number to be used in the design.

If the user of these land patterns desires a more robust process condition for placement and soldering equipment, individual elements of the analysis can be changed to new and desired dimensional conditions. This includes component, board or placement accuracy spread as well as minimum solder joint expectations. In addition, this standard recognizes the need to have different goals for the solder fillet or land protrusion conditions.

Dimensions that have had their tolerance spread reduced are so indicated in the tables. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Tables 13-2 through 13-12 indicate the principles used for three-land pattern goals. The tables reflect maximum, median and minimum material conditions for the land protrusions used to develop the land pattern used to mount various lead or terminations of components that are to be surface mounted.

Table 13-2 Flat Ribbon L and Gull-wing Leads (Greater than 0.625 mm Pitch)

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	1.0	0.65	0.2
Heel	0.5	0.35	0.2
Side	0.1	0.05	0.03
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.5	Nearest 0.05

13.4.1 Land pattern Configurations for Small Outline Packages Defined in IPC-SM-782. The SOT-23 package is the most common three-leaded surface mount device configuration. SO-89 packages are used for high power devices where heat transfer to the supporting printed board is important.

With a SOT-23, the single land on one side of the package can be enlarged when reflow soldering is used, so that the

Table 13-3 Round or Flattened (Coined) Leads

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	1.0	0.65	0.2
Heel	0.5	0.35	0.2
Side	0.1	0.05	0.03
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.5	nearest 0.05

Table 13-4 J-Leads

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	0.2	0.2	0.2
Heel	1.0	0.7	0.4
Side	0.1	0.05	0.0
Courtyard excess	1.5	0.8	0.2
Round-off factor	Nearest 0.5	Nearest 0.5	Nearest 0.05

Table 13-5 Rectangular or Square-End Components (Ceramic Capacitors and Resistors)

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	1.0	0.4	0.2
Heel	0.2	0.1	0.0
Side	0.2	0.1	0.0
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.05	Nearest 0.05

Table 13-6 Rectangular or Square-End Components (Tantalum Capacitors)

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	2.0	1.0	0.2
Heel	0.0	0.0	0.0
Side	0.2	0.2	0.2
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.05	Nearest 0.05

Table 13-7 Cylindrical End Cap Terminations

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	1.0	0.4	0.2
Heel	0.2	0.1	0.0
Side	0.2	0.1	0.0
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.5	Nearest 0.05

Table 13-8 Bottom Only Terminations

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	0.2	0.1	0
Heel	0.2	0.1	0
Side	0.2	0.1	0
Courtyard excess	0.25	0.1	0.05
Round-off factor	Nearest 0.5	Nearest 0.05	Nearest 0.05

Table 13-9 Leadless Chip Carrier With Castellated Terminations

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	1.5	1.25	1.0
Heel	0.4	0.2	0.1
Side	0.0	0.0	0.0
Courtyard excess	1.5	0.8	0.2
Round-off factor	Nearest 0.5	Nearest 0.5	Nearest 0.05

Table 13-10 Butt Joints

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	2.0	1.0	0.6
Heel	2.0	1.0	0.6
Side	0.3	0.2	0.1
Courtyard excess	1.5	0.8	0.2
Round-off factor	Nearest 0.5	Nearest 0.5	Nearest 0.05

Table 13-11 Inward Flat Ribbon L and Gull-Wing Leads

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	2.0	1.0	0.2
Heel	0.0	0.0	0.0
Side	0.2	0.2	0.2
Courtyard excess	0.5	0.25	0.05
Round-off factor	Nearest 0.5	Nearest 0.5	nearest 0.05

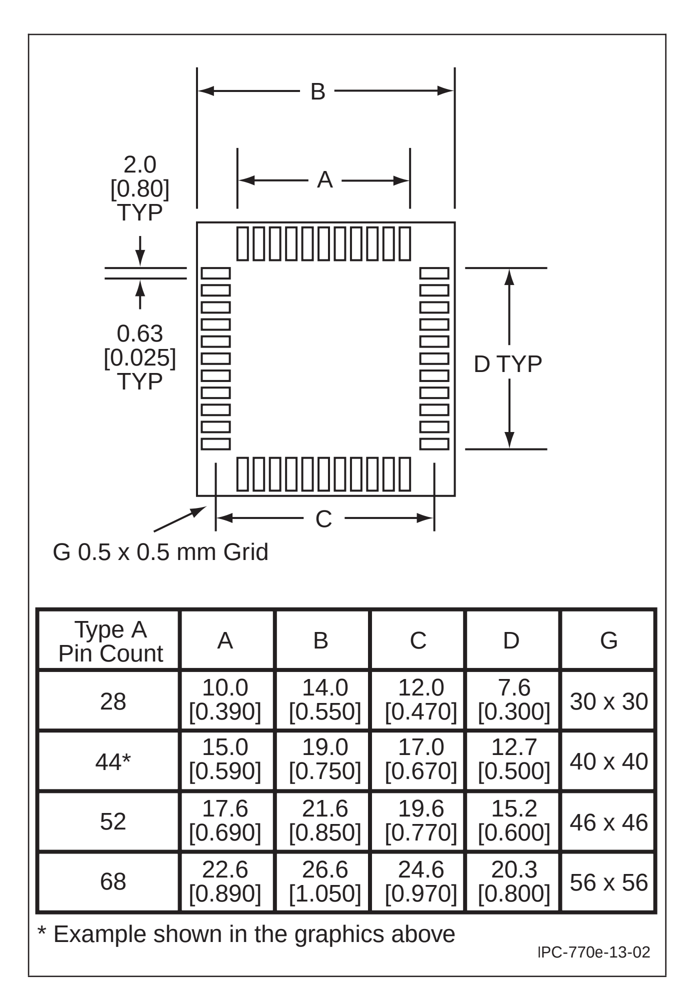
Table 13-12 Flat Lug Leads

Lead Part	Maximum Level 1	Median Level 2	Minimum Level 3
Toe	2.0	1.0	0.5
Heel	0.0	0.0	0.0
Side	1.0	0.5	0.3
Courtyard excess*	2.0	1.5	1.0
Round-off factor	Nearest 0.5	Nearest 0.5	nearest 0.05
*Depends on thermal requirements			

solder-lead surface tension is more nearly balanced. When wave soldering is used the parts are held onto the board with an adhesive and the surface tension balance is not important.

13.4.2 Land patterns for DIPs and SIPs DIPS and SIPS that are surface-mounted depend on the lead shape of the parts. The gull wing lead shape uses the same land pattern concepts for SOICs. When using DIPs with the ''I''-lead, the land pattern should be sufficient to provide a minimum of 0.25 mm on all sides of the lead.

13.4.3 Chip Carrier Land Patterns The land patterns used with chip carriers fall into two main categories: high density and low density. These categories are based on the local routing density associated with the surface mounted device. The selection, design and position of the land geometry in relation to the chip carrier have a significant impact on the resultant solder joint configuration. An example of a land pattern is presented in Figure 13-2 for use with Type A leaded chip carriers (see IPC-SM-782).



Type A Pin Count	A	B	C	D	G
28	10.0 [0.390]	14.0 [0.550]	12.0 [0.470]	7.6 [0.300]	30 x 30
44*	15.0 [0.590]	19.0 [0.750]	17.0 [0.670]	12.7 [0.500]	40 x 40
52	17.6 [0.690]	21.6 [0.850]	19.6 [0.770]	15.2 [0.600]	46 x 46
68	22.6 [0.890]	26.6 [1.050]	24.6 [0.970]	20.3 [0.800]	56 x 56

* Example shown in the graphics above

IPC-770e-13-02

Figure 13-2 Chip Component and Lands

The attachment lands for surface mounting leadless chip carriers should be the same width as the component terminal maximum plus 1.3 mm whenever possible. The land length should extend between 3.8 to 1.0 mm beyond the maximum chip carrier outline on each of all four sides to create a horizontal solder fillet length equal to the vertical fillet rise.

13.4.4 Land Patterns for Surface Mount Connectors The size of the land on the board is directly related to the size of the lead to be soldered plus a tolerance needed to adapt to any inaccuracies in placement. Generally, a land that is 0.25 mm larger on all sides than the lead is recommended. The minimum land size must be sufficient to provide a fillet on all sides of the lead.

13.4.5 Land Patterns for Surface Mount Sockets Surface mount sockets for the most part have the terminals folded under the insulator, making it difficult to visually align the densely populated terminal to the conductor pattern. As a consequence, certain suppliers have provided alignment holes in the chip-mounting cavity to align the socket to either special nonfunctional lands or holes. An adhesive is usually utilized under the body to hold the socket in position prior to soldering. Socket land patterns are normally identical to the device land pattern in order to retain consistency but allow a socket option. A typical land pattern is shown in Figure 13-3.

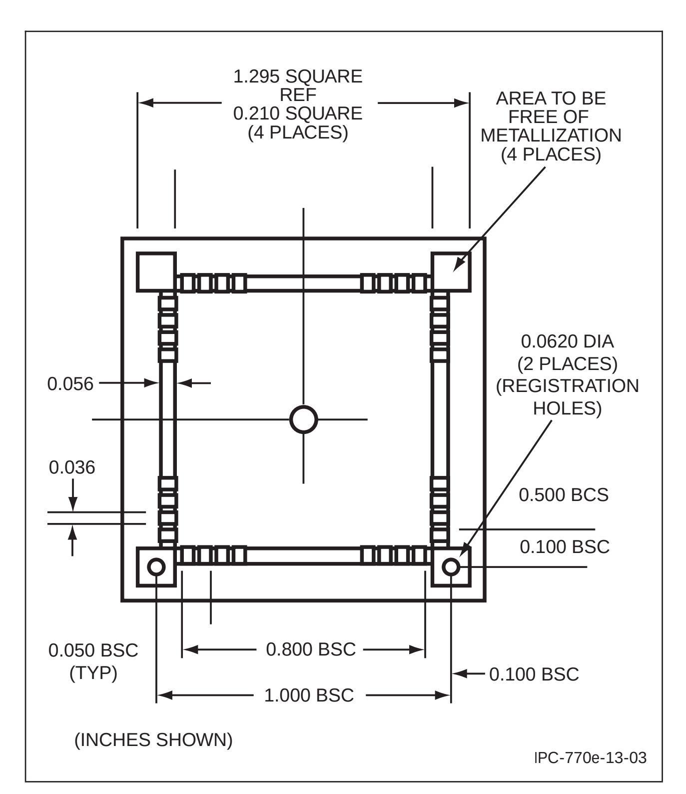


Figure 13-3 Example of 68 I/O Land Pattern on Printed Board Structure

13.5 Alternative Printed Board Structures

13.5.1 Supporting-Plane Printed Board Supporting metallic or nonmetallic planes can be used with conventional printed boards or with custom processing to enhance

printed board properties. Depending on the results desired, the supporting plane can be electrically functional or not and can also serve as a structure stiffener, heatsink and/or CTE constraint.

13.5.2 High-Density Printed Board Technology High-density, sequentially processed, multilayer printed board structures are available with organic dielectrics of specific thickness, ultra-fine conductors, and solid plated vias for layer-to-layer interconnections with thermal lands for heat transfer, all connected to a low-CTE metal support heat-sink. Thus, this technology combines laminating materials, chemical processing, photolithography, metallurgy, and unique thermal transfer innovations, such that it is also appropriate for mounting and interconnecting unpackaged integrated circuit chips.

The major advantage of this system is that the vias can be as small as 0.10 mm or less and conductor widths can range from below 0.12 mm for high interconnection density. Some applications can be satisfied with fewer signal layers while providing additional layers for power and ground.

13.6 Surface Preparation Abrasives, knives, scrapers, emery cloth, sandpaper, sandblasting, steel wool and other abrasives should not be used on surfaces to be soldered. Leveling of solder-coated surfaces on a board using a rotating stainless steel brush is permitted provided the surface is thoroughly cleaned to remove slivers of solder and the board is assembled within three working days.

13.6.1 Temporary Masking Guidelines Temporary masking is used to prevent solder filling printed through-holes (PTHs) or vias, or to protect surfaces not to be coated with solder. The guidelines are:

- Total surface area to be protected should be covered with maskant.
- Any residues from the temporary adhesive should not reduce the cleanliness or the solderability of the protected areas.
- Subsequent processes should not be adversely affected.

13.7 Gold on Printed Board Surface Mount Lands Where immersion or other gold coating has been applied as a solderable surface finish on a printed board.

13.7.1 Gold Thickness Gold thickness should not be sufficient to cause gold embrittlement in the soldered joint. In most applications, this is achieved when the coating is <0.15 µm thick, typically between 0.03 µm and 0.05 µm.

It is sufficient to demonstrate by calculation that there is less than 3% by weight or 1.4% by volume of gold in the solder joint.

For high reliability products containing leaded surface mount components, the calculation should assume that all the gold is present in the region immediately beneath the lead, ignoring heel and edge fillets.

Any barrier layer beneath the gold should not, by diffusion through the gold, reduce the land solderability.

13.8 Printed Board Condition To assist in maximizing printed board solderability and flatness, the following guidelines should be used:

- The printed board surface finish and the method and date of applying it should be confirmed as suitable for the soldering process to be used.
- The flatness of the printed board material and the flatness of the solder coating should be confirmed. A determination should be made that the surface finish is suitable for the components to be mounted thereon, for the assembly equipment, and the soldering process(es) to be used.
- Where gold flash solderable surfaces are used, the gold plating thickness should be in accordance with 13.7.1. Any preflux or anti-oxidant coatings applied to the board should be confirmed as being acceptable for the intended assembly process sequence. Check that such coatings are suitable for assemblies requiring more than one pass through a mass soldering machine.
- All printed board solderable surfaces should be clean and free from detritus and contamination.

14 SURFACE MOUNT

14.1 Assembly Hierarchy

14.1.1 Sequence The selection of a particular method for mounting and connecting components in equipment depends on the type of component package involved; e.g., the equipment available for mounting and interconnecting; the connection method used (soldered, welded, crimped, etc.); the size, shape, and weight of the equipment package; the degree of reliability and maintainability (ease of replacement) required; and on cost considerations. Refer to IPC-D-279 for DfR recommendations.

14.1.2 Attachment Issues When surface mounting, good solderability of chip component terminations is essential for high assembly yield. The solderability of the end terminations should be tested on all new components upon receipt and after any prolonged storage (longer than one month).

The preferred termination can be reflowed or dipped only if excess solder is removed from the end terminations. Bare silver-palladium terminations should be avoided because such terminations tend to lose solderability when exposed to a solder bath or any other large volume of solder.

Component terminations should have a diffusion barrier layer (typically nickel or copper) under the solder to prevent the leaching of silver from the underlying silver-palladium termination. No silver should be detectable on the surface of the component.

Conductors can be connected to a land at any portion of the land perimeter but vias should not be located on or in contact with the land, except when blind vias are used. However, when reflow soldering is used, conductors should be covered with solder resist to minimize scavenging of solder away from the component termination. This is especially important when conductors connect to plated-through-holes near the component termination land.

14.1.2.1 Through-Hole Mounting Chip components are normally leadless or have ribbon leads that are not appropriate for through-hole assembly. SO devices are not designed for through-hole mounting.

In general through-hole mounting does not apply to chip carriers. However, in some cases, leaded chip carriers utilize clip type leads designed for through-hole mounting.

Leaded-type A and all leadless-type chip carriers can be interconnected to the printed board using through-hole mounted sockets. There are some advantages to this approach including simplified replacement of the chip in the event of failure or design change and reduced exposure of the chip to damage during assembly and soldering.

14.1.2.2 Surface Mounting Surface mounting is a technique applicable to most component types, and is used for a variety of reasons. The technique was developed and proven for stripline and other high frequency applications where lead placement and discontinuities had to be strictly controlled.

The technique was found to be a reliable and viable solution to a number of problems, and is now in wide use.

Surface mounting consists of placing the component on the printed board or other suitable substrate, and making the necessary electrical connection to the component on the same side of the board. The leads of surface mounted components do not pass through the board to make electrical connections. The specific connection technique to be used depends on several factors.

In general, leaded components are lap-soldered to the terminal areas, while solder fillets between a solderable area on the component and the land area attach leadless components.

Orientation and placement of components on the ''solder side'' of the assembly should be such that bridging or depleted solder on the following component does not occur (see Figure 14-1).

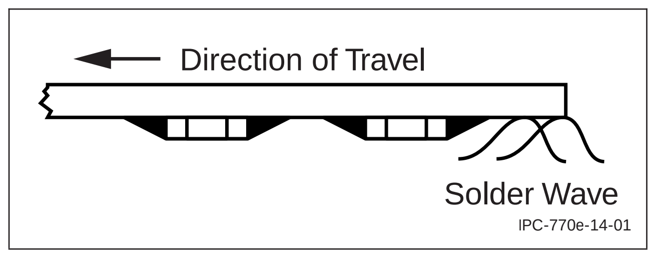


Figure 14-1 No Bridging

14.1.2.3 Lead Forming General guidelines for lead extension and forming for leaded components are illustrated in Figure 14-2. When formed, the leads must be held close to the body to prevent damage to seal.

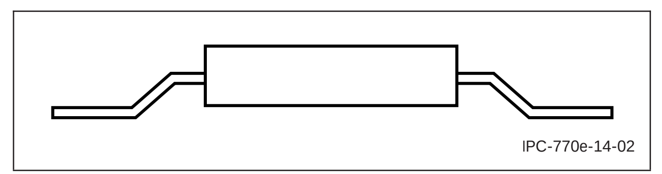


Figure 14-2 Lead Forming for Surface Mounting

Leaded components should be mounted with the body. The minimum distance above the surface should be 0.25 mm except when the part body is sealed to the surface of the board with adhesive so that no flux, moisture, or other contaminants can become trapped. Round axial leaded parts need not be elevated, since the body configuration permits thorough cleaning.

A major consideration in using leaded components is to assure that all leads are coplanar. A tolerance of +0.05 mm is recommended to assure adequate solder filleting to each lead.

Alternative definition: use the three longest noncollinear leads to define a plane (sit the part on a flat surface) then all leads should be within +0.05 mm of the surface.

It should be noted that the JEDEC standards do not contain such a stringent coplanarity requirement. Therefore, lead forming by the user is usually required.

Lead forming is not applicable to leadless components. Solderability, however, is of prime importance. All surfaces to be soldered should be pretinned and verified as very solderable through one of the recognized solderability test methods, such as J-STD-002.

The formed leads should be parallel and in contact with the lands on the mounting base without unplanned overhang. The maximum angle that is allowed between the lead pad and parallel-mounting base is 15°.

14.1.2.4 Lead Support Leads should be supported during forming to protect lead to body seal.

14.1.2.5 Coined Leads Round cross-section leads usually are coined to enhance mounting stability. Components

with axial leads of round cross section should be utilized for planar mounting only if the leads are coined or flattened for positive seating.

14.1.2.6 Component Support Depending upon weight, components can be secured for soldering in the following ways:

- For light components, solder paste with relative high solid content can be used to hold pretinned lead and land together.
- For heavier components, adhesive or mechanical means can be used.

14.1.2.7 Metallurgical Considerations The general requirement for cleanliness and solderability of terminations on all components is of utmost importance in the case of both leadless and leaded chip carriers. Inspection, repair and rework of soldered surface mount component assemblies are in general more complex than that for through-hole mounted components. Frequent socketing of chip carriers requires that they have appropriate contact metallurgy to aid in insuring a reliable electrical interconnection.

Pretinning of leadless chip carrier metallizations enables evaluation of solderability characteristics prior to assembly. The additional solder volume improves joint shear strength.

Chip carriers can have mold release on the leads and may need to be cleaned with an appropriate solvent prior to lead attachment for improved solderability.

14.1.2.8 Mechanical Considerations Chip carriers that are initially leadless can be used with the addition of clip leads for surface mounting. Clip leads are available with or without solder preforms in the attachment areas, and the leads afford a compliant member between the chip carrier and substrate (see Figure 14-3).

Leads can be mechanically attached in strip form with tooling, which ensures proper seating and alignment with the terminal metallization. The leads can then be soldered to the chip carrier by an appropriate reflow method or, if the leads are supplied with solder preforms, the soldering of the leads to the chip carrier can be done simultaneously with the attachment of the chip carrier to the substrate. In the former case, all residues should be removed by cleaning with a flux-removal solvent prior to the final mounting of the chip carrier. Coplanarity of leads is critical to reliable soldering of the mounted components. Coplanarity should be kept to +0.05 mm. Accurate repeatable preparation of leaded chip carriers is necessary. It is also necessary to protect the leads from distortion prior to assembly. Good planarity is required to ensure that the lead ends make adequate contact with substrate solder lands. Flatness of the substrate is also of concern and needs to be controlled.

When the decision is made to use through-hole components in combination with surface-mount components, some of the advantages of a totally surface mount assembly are compromised. Through-hole components can be modified for surface mounting, but modified components do not result in the space savings surface mount components provide.

14.1.2.9 Small Outline Devices Manufacturers supply small outline (SO) devices with leads preformed for

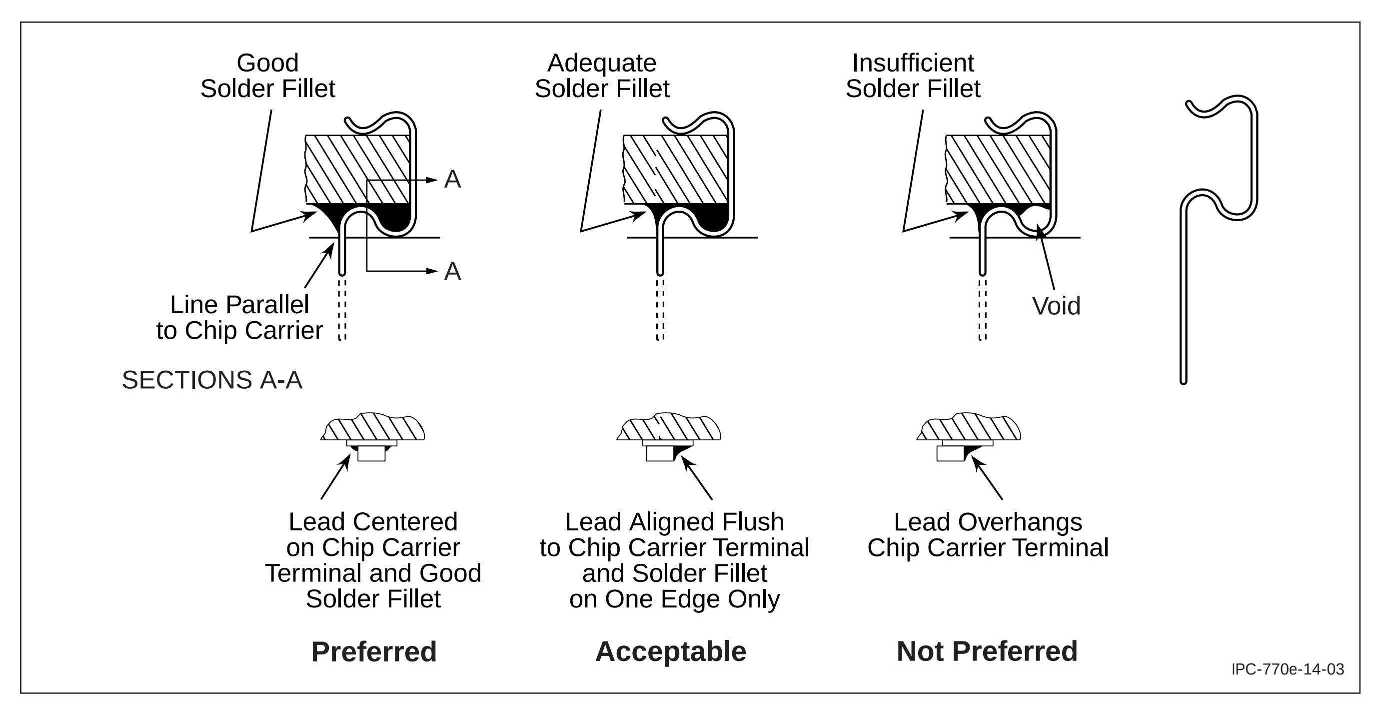


Figure 14-3 Criteria for Lead Attachment to Leadless Type A (Leaded Type B)

surface mounting. Lead configurations are illustrated in Figures 14-4 and 14-5.

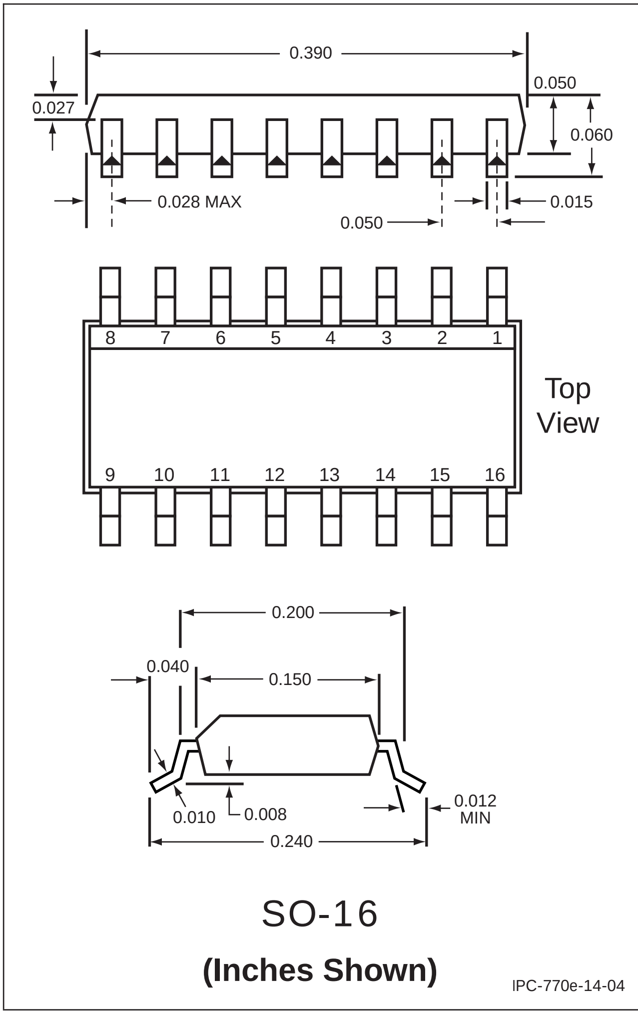


Figure 14-4 SO-16 Package Drawings Typical Dimension

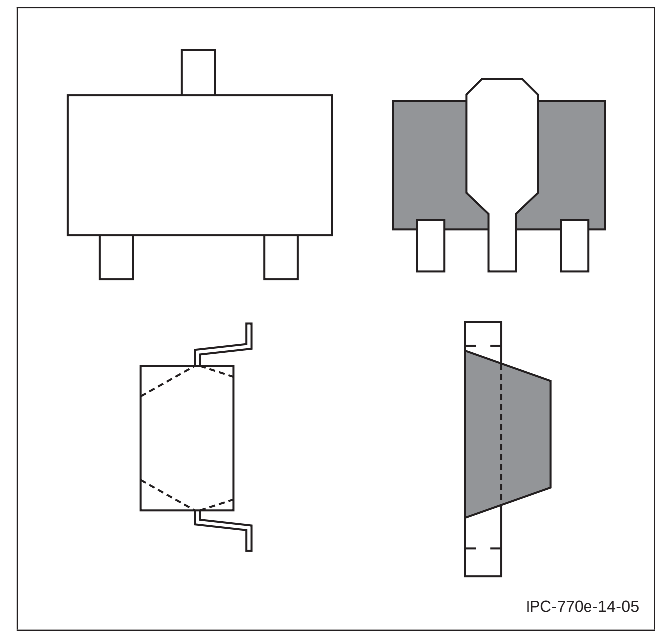


Figure 14-5 Typical SOT Packages

14.1.2.10 Component Lead Preparation One method for surface mounting both through-hole and surface-mounted components on the same board is to modify the through-hole component leads so that they can be surface-mounted and soldered.

14.1.2.11 DIPs When only a few DIPs are involved on an otherwise surface mounted assembly, the leads can be formed to resemble a SOIC package (see Figure 14-6).

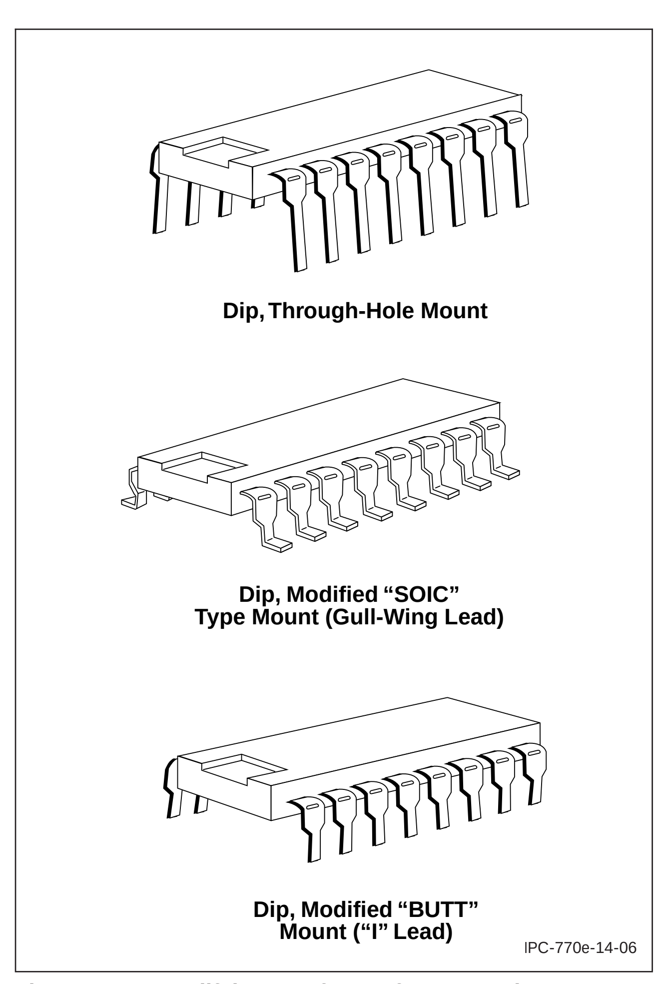


Figure 14-6 Modifying DIP for Surface Mounting

For production, machines are available which cut and form IC leads into a ''gull wing''-type configuration (see Figure 14-6).

Another method of modifying DIPs for surface mounting is the ''butt'' mounting technique. This involves simply cutting the DIP leads to a shorter length and placing the device on a land pattern to be soldered along with the other surface mounted devices.

14.1.2.12 SIPs SIP lead forming is shown in Figure 14-7. Care should be taken to assure coplanarity of the reformed leads, especially if the assembly is to be vapor phase reflow soldered. Leads can be carefully formed by hand for low volume or prototypes. For production, machines are available which cut and form IC leads into SOIC type configuration.

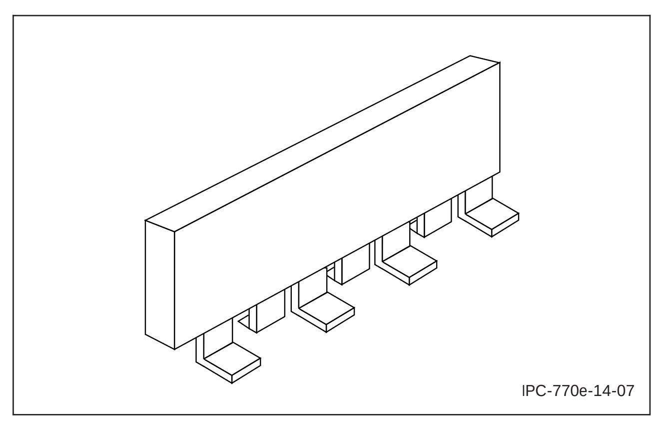


Figure 14-7 Gull-Wing Lead for SIP-Type Component

14.1.2.13 Surface-Mount Connectors Surface mount connectors are designed with compliant leads that are usually reflow soldered to the lands located on the surface of a board. Although not as popular, alternate methods of attachment at the nonseparable interface include pressure and conductive epoxy. Connectors designed for surface mount carry the implicit qualities associated with high-temperature, dimensionally stable materials. Examples of surface mount connectors are shown in Figures 14-8 through 14-11.

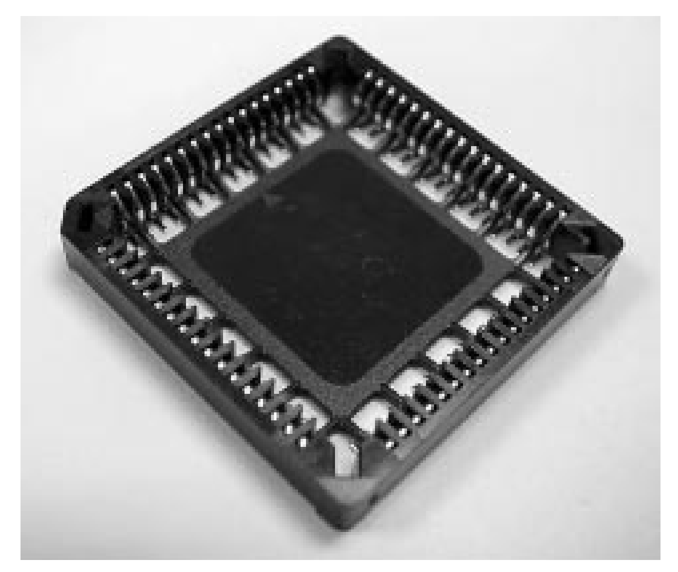


Figure 14-10 Surface Mount Receptacle

Connectors for surface mounted substrates differ from through mounted connectors in the following ways:

- The plastic insulator material must be chosen to withstand the high temperatures (215°C) encountered during reflow solder processes.

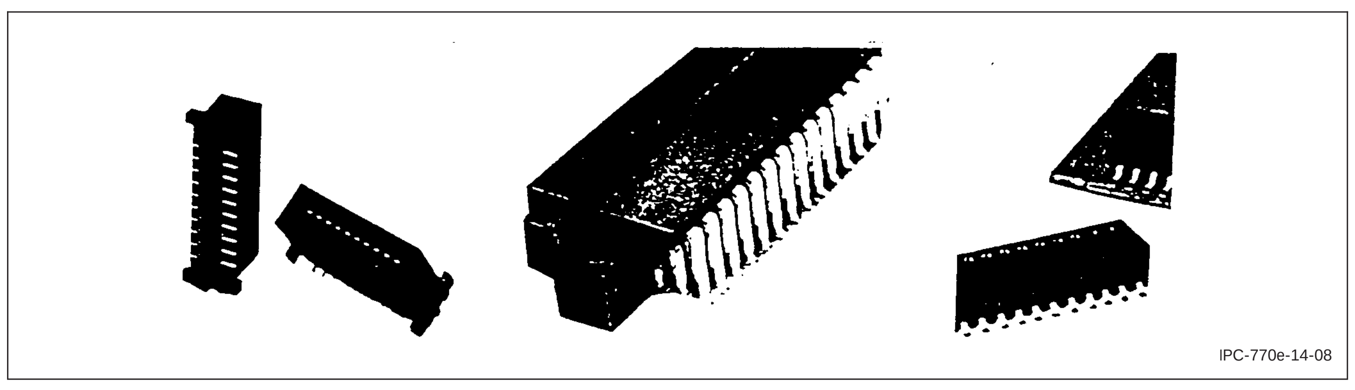


Figure 14-8 Surface Mount Connector

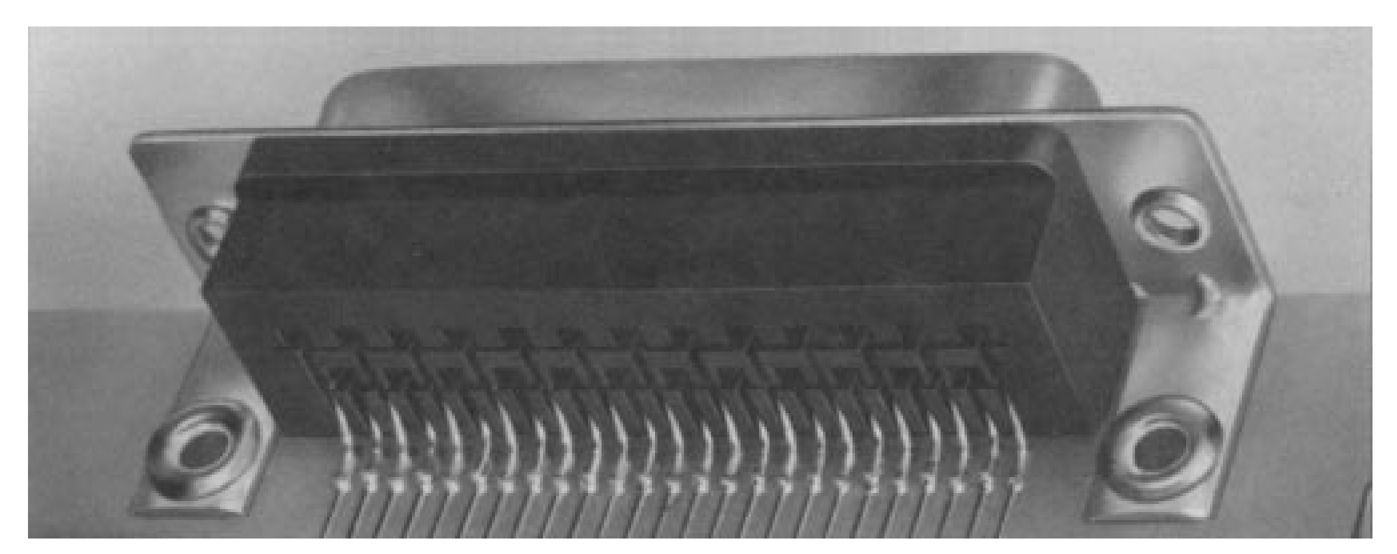


Figure 14-9 D-Subminiature Surface Mount Connector

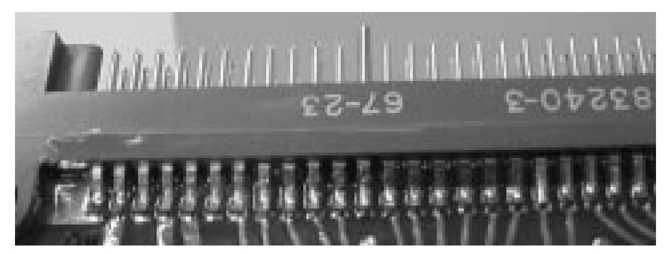


Figure 14-11 Box-Contact Surface Mount Connector

- The leads have been formed to make contact with the lands on the board. The more intimate the contact is between lead and land, the better.
- The leads should be plated so as to assure good solderability to the land. Solderability of leads can be checked using simple tests described in J-STD-002.
- The connectors can require features for mechanical attachment to the board. This is especially desirable for longer connectors or connectors that are potentially subjected to abuse during mating and unmating.

Alternative methods of surface mounting include the use of pressure contacts to maintain electrical contact at the board, and the separable interface. A point in these applications is the need to provide board-stiffening structures to neutralize the effect of ''normal'' forces.

An evolving technology is the use of conductive epoxies to surface mount a connector to board. Utilization of this method affords the potential of lower processing temperatures.

Extra care should be taken with surface mount connectors to assure that the leads are not damaged prior to placement on the board.

Care must be taken so that flux or solder does not wick up into the contact. Some manufacturers provide anti-wicking devices to prevent flux or solder wicking. If connectors are not mechanically secured to the board, suitable fixturing should be provided to prevent lifting during soldering. This is especially important with small lightweight connectors.

14.1.2.14 Surface Mount Socket Instead of straight solder tails, which are inserted into through-holes, the surface mount socket has flat ''L'' or ''J'' type leads.

Figure 14-12 shows a section through a contact that can be used with the type of socket in Figure 14-13 to provide for surface mounting. This contact has a long compliant lower leg and mates with the land pattern shown in Figure 14-14. The two registration holes mate with corresponding projections on the socket.

Figure 14-15 shows an alternate contact configuration. At the cost of reduced compliance, this contact has a shorter electrical path, allows an easier visual inspection of the soldered joint, and requires a different land pattern.

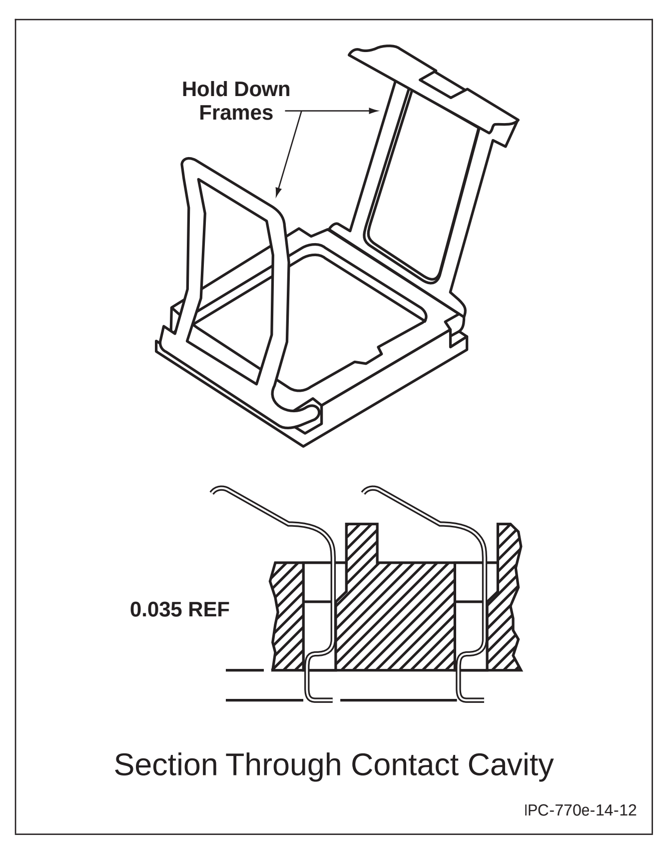


Figure 14-12 Leadless Grid Array Socket

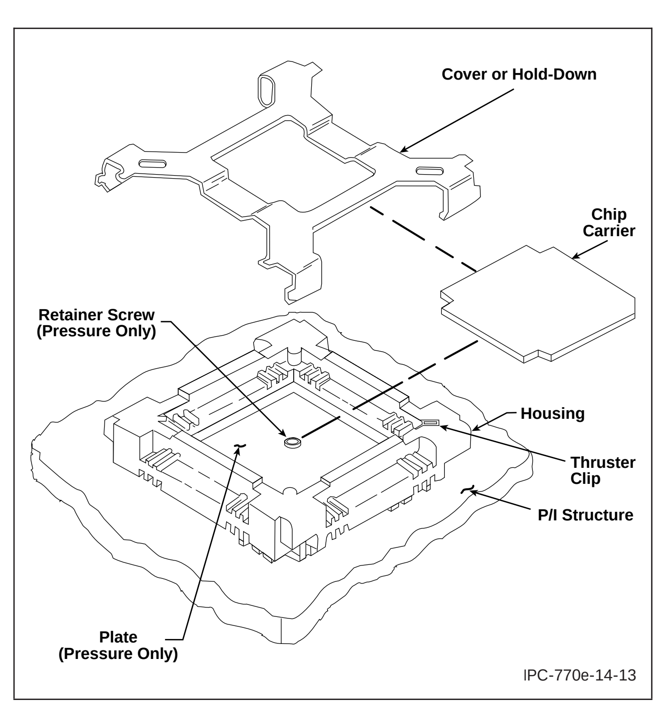


Figure 14-13 Surface Mount Chip Carrier Socket

For sizes larger than the 68-position (1.27 mm) centerline, the interaction of the contact force and cover force can distort the connector housing. This can, in turn, strain the solder joint.

This situation is avoided by use of the four corner screws to engage a backup plate. These transfer the forces from

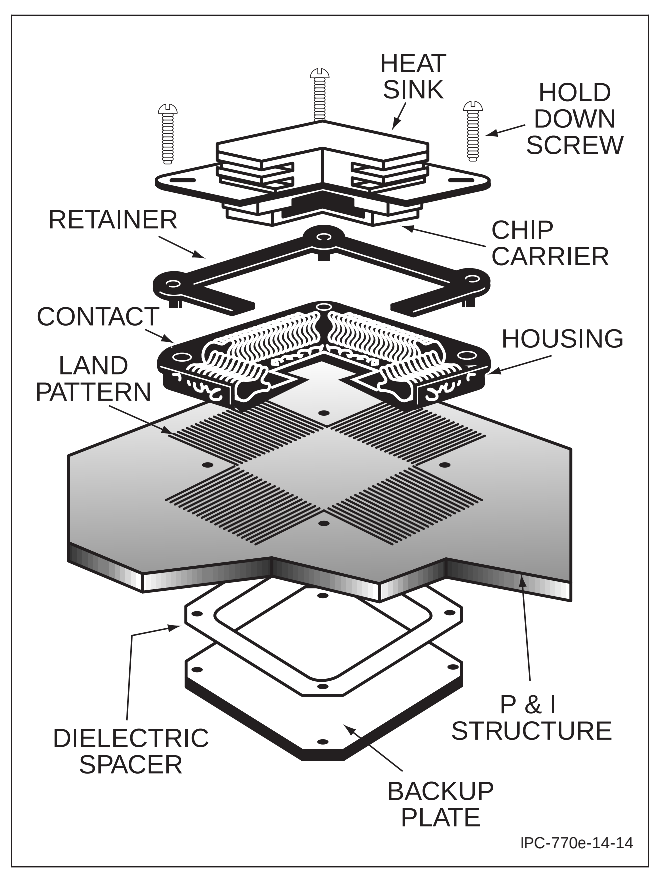


Figure 14-14 High Speed Circuit Socket

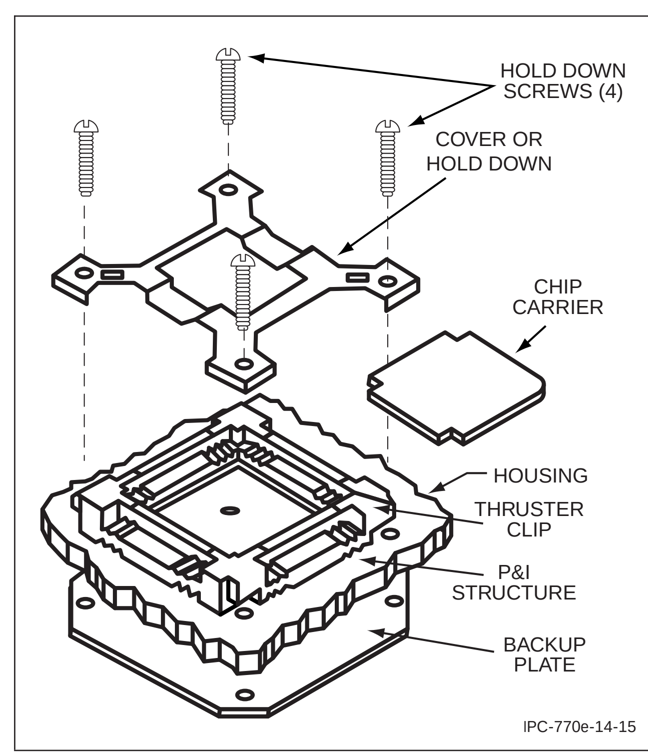


Figure 14-15 Screw Down Cover

the cover to the backup plate and establish the closed system that minimizes the forces on the housing, the printed board structure and the solder joints.

A thruster clip is used to bias the leadless type A, B or D chip carrier into a zero reference position for good registration. The hold-down has compliance to accommodate the thickness tolerance of the chip carrier (CC). It snaps into place and retains the CC. An opening is provided to accommodate a heat sink.

The type of socket shown in Figure 14-13 can also be obtained with a mechanical contact pressure interface with a printed board structure. The advantages of this type of socket are the ease of replacement of the socket in the field. The disadvantage is that a second mechanical interface is now in the circuit. Figure 14-16 shows how the socket is mounted on the structure. Two alignment/locating pins in the socket engage two mating holes on the printed board structure. The pins serve as registration as well as polarizing devices. A screw clamps the socket to the structure by means of a backup plate and a socket plate. The clamping action of the screw and plate causes the lower half of the contact to deflect and generate the contact force. This arrangement is suitable for 68-position (1.27 mm) centerlines and smaller. In the larger sizes, the contact force becomes too great for a single screw clamp. Four corner-clamping screws are used in the larger sizes.

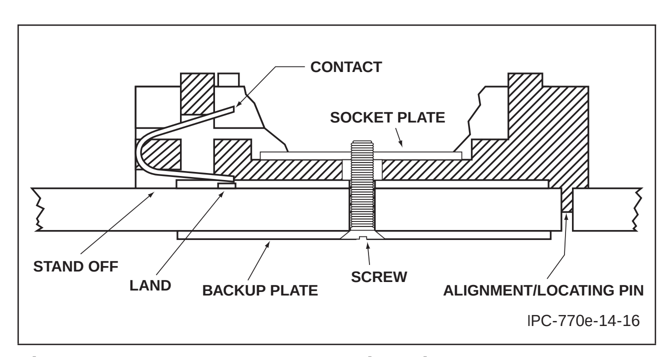


Figure 14-16 Pressure Mounted Socket

The center screw is used to hold the socket in place until the four corner screws are engaged. The center screw applies a preload to the bottom beams of the contact. After the chip carrier is inserted into the socket, the four corner screws secure the cover. These corner screws are torqued until the full contact load is developed. The load is transferred to the backup plate, reducing the load on the printed board structure and minimizing creep under load.

14.1.2.14.1 Soldering Considerations for Surface Mount Socket Due to the terminal/contact configuration, sockets have a tendency to sink more heat than other components. As a consequence, they require a slightly longer dwell time. Due to inability to adequately clean terminal area, the user/manufacturer can restrict the use of activated fluxes. In wave soldering through-hole mounted sockets, the socket must be mounted on the component side of the printed circuit board or carrier. Care must be taken to ensure that flux or solder does not wick up into the receptacle area of the socket.

14.1.3 Lead/Land Configuration after Assembly

14.1.3.1 Small Outline (SO) Devices can be mounted with or without adhesive. If adhesive is used to secure the SO package to the substrate, major considerations are:

- The adhesive must not contaminate the land area. (Refer to Section 3 and J-STD-004.)
- The adhesive must be cured prior to soldering.

14.1.3.2 Lead Configuration for Surface Mounting of SIPs and DIPs The configuration remains the same after assembly as before assembly. If reflow-soldering techniques are used, the leads must be in contact with the solder paste, the fused tin/lead plating or the solder coating on the lands. Proper handling is required so components do not move prior to the reflow soldering operation.

14.1.3.3 Lead/Land Configuration after Assembly for Chip Carriers Care must be taken to assure the condition of the chip carrier terminations is such that solderability is not adversely impacted. Techniques in storage, handling and placement must be adequate to preserve good metallurgical and mechanical properties of the termination up to and through placement of the device.

14.1.3.4 Mounted Component Configuration Device performance, quality, reliability, solder joints and the ability to withstand operating environments are, in part, dependent on control of the configuration of the mounted component/substrate interface.

Assembled chip carriers can be constrained mechanically or with adhesive prior to soldering, or they can be allowed to float. If adhesives are used, they should not absorb moisture, create a conductive leak path or interfere with solder joint formation. Standoffs can be used to control solder joint configuration and/or provide required clearance for cleaning after solder. It is generally recommended that a clearance of 0.25 mm minimum be provided between the chip carrier and the substrate to facilitate adequate cleaning.

In some solder paste applications, the leadless components can be allowed to ‘‘float’’ because surface tension serves to pull the chip carrier into correct alignment with respect to the land pattern. However, this is dependent upon chip carrier size, positional tolerance, flatness of leads, etc.

For leaded chip carriers having through-hole clip leads, adequate tooling should be used to assure the leads mate with holes in substrate. Preforms can be used on either side, depending upon structures and orientation during reflow.

14.1.3.5 Surface Mount Connector Lead/Land Configurations after Assembly Surface-mount connector leads are not reconfigured after surface mounting. The location, or true position, of component leads becomes more critical as the number of inputs/outputs increase. Board hole tolerances and lead tolerances over the length of some of the larger connectors can cause interference problems when mounting. In such instances, mounting aids are required and are provided by the connector manufacturer. An important consideration with larger surface mounted connectors is the difference in thermal expansion between the connector plastic and the printed board. All commonly used plastic materials have a coefficient of thermal expansion (CTE) that exceeds that of epoxy glass boards by at least 7 ppm/°C (17 ppm/°C for ceramic substrates). The mechanical connector design must be able to absorb this CTE difference to avoid solder joint failures during thermal cycling. Visual examination of leads of the mounted connectors is recommended. Reposition individual leads if required.

14.1.3.6 Surface Mount Socket Component Preparation Lead forming is not performed on surface mount sockets.

14.1.4 Placement

14.1.4.1 Mounted Component Configurations When design criteria permits, chip components to be wave soldered should be oriented such that the longitudinal axis of the chip components (a line passing from the center of one termination to the other) is perpendicular to the direction of motion through the wave so that the two terminations meet the wave at the same time. Chip components that pass longitudinally through the wave can generate ‘‘no-solders’’ or insufficient solder joints on the following termination. Adequate space must be left between adjacent components and between components and other board features to avoid shorting or bridging during soldering.

14.1.5 Mixed Technology Chip components are commonly assembled to boards where both surface mount and through board mount components are used. Frequently the chip components are attached to the ‘‘solder side’’ of the board with adhesives and soldered to the lands at the same time as the through board components by passing through a solder wave. Chip components that are to be wave soldered must be qualified for immersion in molten solder.

Alternatively, the chip components can be attached on the ‘‘solder destination side’’ of the board with solder paste (and sometimes with adhesive to guarantee mechanical attachment) and reflow soldered to the mounting lands. After the reflow soldering of the surface-mount components, the through-board mounted components are wave soldered. The wave soldering process should not melt the surface mount joints on the top of the board.

Higher pin count SO devices are normally mounted on the component side of the substrate, while the small SOT devices can be found on both sides.

The process sequence for mixed assembly using chip carriers varies depending on what type of other components are mounted on both sides of the substrate, and what specific solder process (or processes) is used.

Where through-hole mounted components and discrete chips and chip carriers are all mounted on the same side of the board, the order of assembly must take into account the solder process to be used. As for class C-1 assemblies, if solder preforms are utilized with the through-hole mounted components one of the solder passes can be eliminated.

14.1.5.1 Surface Mount Connector Mixed Technology These assemblies generally are wave soldered as the last attachment step. Standard through-hole connectors can therefore generally be used for mixed assemblies. These connectors should be applied after the reflow solder process or must be chosen to be compatible with the high temperatures seen during reflow soldering.

14.1.5.2 Surface Mount Socket Mixed Technology Few considerations apply to mixed assembly. The assembly sequence is normally dictated by the soldering procedures to be used. Sockets are not intended for direct immersion in solder, therefore are restricted to the component side of the printed board or carrier when the assembly is to be wave soldered. For solder flow processes the socket insulator material must be compatible with the reflow process.

Sockets in today's packaging schemes are being used for increasingly specialized applications and therefore sockets are used less frequently. As a consequence, sockets appear more often in mixed mounting situations. Several physical points arise unique to sockets:

- ***Heights –*** Although low profile sockets are available, sockets (with their device) present a higher assembly profile. Wave solder holding plates are one-point affected.
- ***Automatic Assembly –*** As sockets are increasingly unique, there can be a tendency to hand load one (or several), which is an anomaly to the board. Designers should be led to reassign socket placement to common boards if possible.
- ***Land Patterns –*** As it is wise to use a device insertion/extraction tool, clearance real estate around sockets is required. The increasing use of chips also necessitates use of a great deal of device I/O patterns that also has a tendency to open board space. These open land areas offer ''hand hold'' and/or probe points that make the board more susceptible to surface damage.

14.2 Manual Techniques Because of the small size of most chip components, manual assembly is limited to low volume production or to designs where only a small number of chip components are to be mounted on each board. Chip components can be handled with tweezers or vacuum pickups and can be manually soldered with a temperature-controlled soldering iron. Manually placed components can also be reflow soldered if the manual placement is properly located in the assembly sequence. Generally, however, manual assembly of chip components to boards is done after all other assembly sequences but before cleaning, inspection and test. Manual assembly techniques are also used in touchup and repair operations.

14.2.1 Manual Assembly Manual installation of surface-mounted components is accomplished in a manner similar to through-hole installation. The exception is greater use of vacuum pick-up devices, which simplify the precise placement of the components, required for satisfactory soldering. Boards designed for manual component installation need not follow the layout guidelines for automatic assembly. However, space must be allowed for exposure to the solder wave (when applicable), test access and rework.

14.2.1.1 Manual Assembly for Surface Mount Connectors Most connectors are inserted or placed using manual techniques. Assembly can occur at the same time as other components or as a separate operation. Care should be exercised to not disturb previously assembled parts.

14.2.1.2 Manual Assembly for Surface Mount Sockets Sockets are normally handled manually using special tools designed for ease of alignment and insertion. On certain sockets a locating pin is used to correctly orient it to the land pattern, such as pressure fit type sockets. Manual assembly as always offers a greater susceptibility to damage. When using these procedures with sockets, the major points to be addressed are:

- ***Board Loading –*** Always load from component side with lands and holes in view. Immediately clinch diagonal terminals on solder side.
- ***Handling –*** Socket contact springs are susceptible to finger oils, handling damage and particulate entrapments. Use of lint free gloves when assembling is appropriate. Handling the sockets with tools or by the insulator is also necessary.
- ***Storage –*** Leads are extremely susceptible to displacement. Remove sockets from the shipping container one at a time and immediately load in the board. Never accumulate/store sockets on the work bench unprotected.
- ***Clipping –*** If leads must be clipped, they should be shortened after they are in the board (never in an unmounted condition).

14.3 Automated Assembly Techniques Most surface mounted components can be assembled using automated equipment. Automated assembly is simplified when the boards are designed for this type of assembly. Figure 14-17 illustrates several considerations that simplify automated

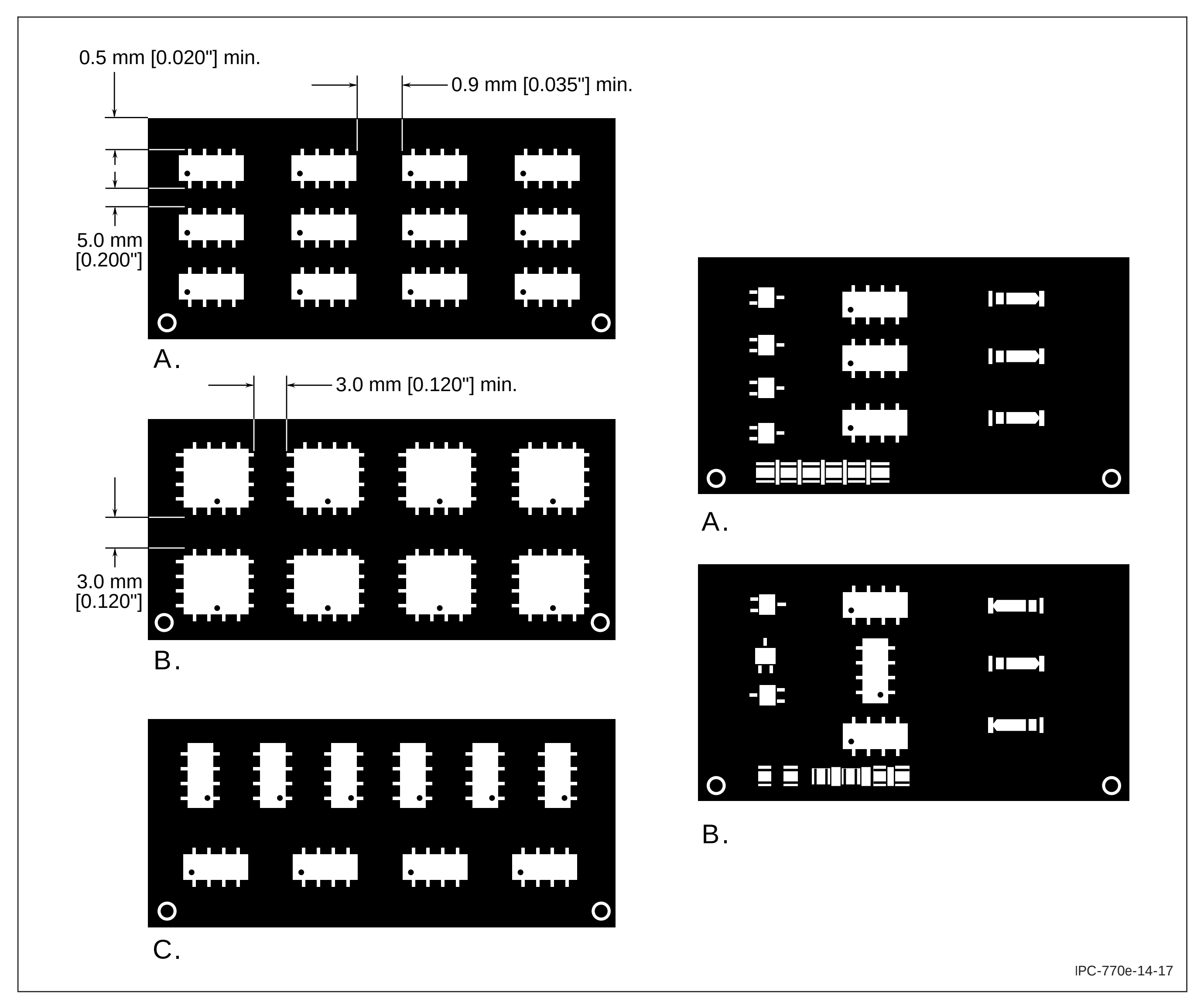


Figure 14-17 Preferred Mounting Orientations

assembly and maximize productivity by restricting table motions.

Chip components are well adapted to automated assembly lines. Fully automated assembly lines for all surface mount products depend heavily on chip component placement for their high throughput. Most chip components are supplied in tape-on reel packaging to interface with automatic placement equipment. The automated placement machines frequently place adhesive dots and then place the chip component on the adhesive for wave soldering processes. When reflow soldering is used, solder paste is screen printed before the parts are placed and the paste is used to hold the chip components in place until the solder is reflowed. Automated board handling facilitates precise and rapid movement of assemblies through the process.

14.3.1 Placement Automated placement techniques applied to high volume, high density mounting of chip carriers provides benefits in quality and productivity.

Currently several manufacturers provide automatic placement equipment and robotic devices to place chip carriers. Robotics can offer more flexibility than other placement equipment while packaging standards are developed. However, placement systems utilizing vacuum pickup and/or self-centering tweezer grips are used today and provide versatility for chip carrier placement.

14.3.2 Automated Assembly of Surface Mount Connectors For many backplane assemblies, computer controlled machines are used which stake individual pins into the backplane. Those pins that are actually needed are staked. Also, pin lengths can be selected for staged mating of ground, power, and signal contacts. Robots are increasingly being used to place connectors. Where robots are being used, it is important to specify connectors with true position tolerances and other key dimensions compatible with the board and robotic placement system. Packaging should also be selected to make delivery of the connector to the robot simple.

14.3.3 Automated Assembly of Surface Mount Sockets Although the bulk of sockets and DIPs can be automatically loaded with stick loaders, the balance do not lend themselves to automation. High board frequency, with a large quantity of sockets, can be loaded by pick and place type equipment. Operation cost, however, must be closely assessed for value.

15 COMPONENT CHARACTERISTICS HIGH PIN COUNT AREA ARRAY

As the performance and speed of microprocessors increases, pin counts increase. This trend continues despite the fact that using multilayer substrates with in-package capacitance for decoupling will electrically enhance these packages. For cost reduction, thermally and electrically enhanced packages are becoming common. For this to happen, however, the industry first must address the reliability concerns in such packages. The complexity of board assemblies increases because packages of varying lead pitches including through hole are used. To reduce board complexity and to increase manufacturing yield, ball grid array packages become common since they reduce process complexity for the user. The suppliers and users both will feel the complexity. Despite complexity in packaging and assembly, the primary driver is cost. So the winners are those suppliers who not only meet the technical challenge to provide a solution, but do so at a continuously decreasing price.

15.1 Component Definition Surface mount grid arrays are pinned (column grid array) or leadless (ball grid array) carriers with I/O contacts that populate the bottom of the package. Surface Mount Ball Grid Array (BGA) packages are considered an alternative to finer pitch, higher I/O packages. The package is typically an overmolded, BT resin glass/epoxy or ceramic substrate. The BGA package distributes the pins-outs over the bottom of the package and is solder assembled to a complementary area array of lands on a printed circuit board. The pin-outs are typically 30 mil diameter solder spheres that are reflowed onto the pads of the package. The use of a solid grid necessitates placing the die cavity on the side opposite the I/O contacts. A double or multiple concentric row grid permits having die cavity and I/O contacts on the same side with an optional heat sink on the opposite side. Some standard types of components are as follows:

- ***CBGA –*** Ceramic Ball Grid Array
- ***PBGA –*** Plastic Ball Grid Array
- ***CCGA –*** Ceramic Column Grid Array
- ***TBGA –*** Tape/Tab Ball Grid Array
- ***MBGA –*** Metal Ball Grid Array
- ***SGA –*** Stud Grid Array
- ***LGA –*** Land Grid Array
- ***FBGA –*** Fine Pitch Ball Grid Array

15.1.1 Body Size Body sizes for Ball Grid Arrays are divided up into the following two groups: square and rectangular.

The square groups have sizes as small as 4 x 4 mm and as large as 50 x 50 mm. In the ranges from 4 x 4 mm to 21 x 21 mm in the fine-pitch variations, sizes change in 1.0 mm increments. In the ranges above 21 x 21 mm, the body size increases in increments of 2.0 to 2.5 mm and the pitches are in the regular range. Rarely are any of the fine-pitch parts found in sizes larger than 21 x 21 mm. Square sizes are normally standardized in large generic families.

The rectangular groups have the same size ranges from 4 to 50 mm but vary with each application. This group can have many more variations than the square group. Rectangular sizes typically are found to follow no fixed incremental progression. This group is normally driven by the memory applications and closely follows the die sizes. Rectangular sizes are normally standardized in small application specific families.

15.1.2 Ball Size Relationships The total variation of the system considers three major issues: positioning, ball tolerance and substrate tolerance. All three attributes added together result in a worst-case analysis. However, as with other land patterns in the standard, a statistical average is determined by using the RMS (root, mean, square) value. Table 4-1 shows the total variation in the system for each of the four ball sizes identified in the standard.

Ball sizes for ball grid packages are controlled by the following requirements: overall package height, package pitch, and solder joint reliability. The solder nominal diameters range from a low of 0.15 to a high of 0.75 mm. The standard ball nominals are 0.15, 0.20, 0.25, 0.30, 0.40, 0.45, 0.50, 0.60 and 0.75 mm. The requirements drive the proper ball selection. The package supplier is always striving to have the best solder joint reliability on the finest pitch, lowest height package. Ball size is a very complex issue and is why ball grid package standardization is so important to the end users; so they know what they are buying.

15.1.3 Coplanarity Another critical issue in surface mount packages is the coplanarity of the leads. The coplanarity requirements in BGA are very different from other surface mount components and, hence, are of great concern to people who have to assemble these packages on the board.

Coplanarity is defined as lying or acting in the same plane. Mathematically speaking, therefore, coplanarity is the distance of component leads above and below a common plane defined as a plane that passes through the average length of all the leads.

This definition is difficult to implement on the manufacturing floor. Thus noncoplanarity, a simplified term, is the

maximum distance between the lowest and the highest pin when the package rests on a perfectly flat surface. This definition represents a package sitting on a PC board on at least three leads.

Even if one lead out of numerous leads is out of an acceptable range, many leads may not solder properly. In the worst case, coplanarity causes open solder joints. The common problem that users encounter because of coplanarity is the phenomenon known as solder wicking. This occurs when solder paste wicks up the lead, causing open solder joints. Poor board or lead solderability or uneven and fast heating during the reflow process can also cause open solder joints.

So a user naturally wants all the lead ends to lay perfectly in the same plane, to avoid manufacturing problems. Component suppliers, however, have a difficult time supplying a perfectly planar package. To satisfy the needs of the users and suppliers, a 100 µm maximum coplanarity has been the standard for surface mount packages. The number for acceptable lead coplanarity is not ± 100 µm or ± 50 µm, but 100 µm maximum, and it should be specified as such in the procurement specification.

There are different coplanarity requirements for different types of BGAs. The following discusses JEDEC's requirements on coplanarity:

- **MO-156/MO-157** Ceramic BGA 0.15 mm
- **MO-158/MO-159** Ceramic CGA 0.15 mm
- **MO-195** Fine Pitch BGA 0.08 mm
- **MO-151** Plastic BGA 0.2 mm

The coplanarity values may vary from JEDEC outline to outline because of the ball metallurgy. In low temperature, eutectic (183°C melting point) solder balls, the balls collapse during the assembly operation, therefore the coplanarity requirement is not as tight as a high temperature (302°C melting point) solder balls in which the balls do not collapse during the assembly operation.

15.2 Component Packaging Style Considerations BGAs fall into two main categories: ceramic and plastic. Ceramic BGAs (CBGAs) have 0.9 mm ball high temperature solder (90% lead, 10% tin) with a melting point of 302°C. The package body is made of multilayer ceramic. Since the ceramic package is relatively very flat, and the tolerances in ball diameters are very tight, the coplanarity requirements can be relatively tight.

A plastic BGA (PBGA) is very different, however, since it is essentially made of circuit board material with high temperature BT (bismaleimide triazine) resin. The balls are made of eutectic solder with a melting point of 183°C (or 179°C for eutectic solder with 2% silver).

These two types of BGAs behave very differently during reflow and have very different consequences for the user and the suppliers. For example, since the CBGA balls do not melt during reflow, solder paste must be applied for joining to take place. In this respect, CBGA is very similar to other leaded surface mount devices such as PLCCs and SOICs where the leads do not melt during reflow and solder paste is necessary for solder joint formation. PBGAs, on the other hand, can be soldered without any solder paste, which is very common.

Circuit board materials have very different warpage requirements. Formerly, 1.5% warpage (15 µm per mm) was considered acceptable for printed circuit boards. Now, for surface-mount assemblies, maximum 0.75% (7.5 µm per mm) warpage is required.

15.2.1 Plastic Ball Grid Arrays (PBGA) The primary driver for fine-pitch is real estate constraint. In addition, there is significant cost saving, in some cases well above 50 percent over PGA. In other cases, such as Intel Pentium for notebook, ultra fine pitch TAB package provides the user a lower profile package necessary for portable computers. Fine pitch plastic package is also a common package for high pin count (over 100) ASIC (application specific integrated circuit) devices. In many cases, ASICs are used for reducing thermal load by combining 10 to 20 programmable logic array devices that would consume 5 to 10 watts into a 2 to 4 watts single ASIC device. These packages allow thermal and electrical enhancements by use of heat slugs and multilayer boards while significantly reducing cost. Package reliability and moisture susceptibility used to be some of the major concerns preventing their wide spread use. However, these issues have been resolved by the industry now. For example, J-STD-020 provides guidelines for classification and handling of moisture sensitive packages.

Because BGAs use solder-bump interconnections instead of leads, problems associated with lead damage and coplanarity are eliminated. Since BGA pitch is in the 1.0, 1.27 and 1.5 mm range, while having over 150 µm of stand-off height, problems with paste printing, placement reflow and cleaning are nonexistent. BGAs also provide much shorter signal paths compared to fine-pitch devices. This feature can be very critical in high-speed applications.

Although BGAs do not require as much rework as fine-pitch devices, many assemblers are apprehensive about packaging expensive silicon in a package that is very difficult to rework. Further costs accrue with the increased board layer counts that BGAs demand. The finer the pitch, the more dramatic the impact is on layer count and board cost.

BGA is not a package suitable for companies that assure quality by inspection and repair. Excluding X-ray and X-ray-like techniques as viable production methods, BGA solder joints cannot be inspected. To reap the benefits that

BGA offers, good process control must be practiced. However, due to limited time and training, many companies find implementing such process control to be a difficult endeavor.

Even if BGA obtains industry and customer backing, suppliers must address some fundamental technical problems: warpage in large BGA packages, higher coplanarity (150 µm, although this issue is not settled) and thermal enhancements in plastic packages for higher wattage devices. Although BGAs can be packaged in ceramic for higher wattage devices, CTE mismatch problems associated with ceramic packages on commonly used glass epoxy circuit boards are a major concern.

However, one can expect the BGA package to be widely used in the future, although at a much slower pace expected. BGA is to be used first in low-cost packages where there is no cost penalty for using this new technology (right now BGA costs more). When users stop worrying about the potential of throwing away a functional package because of rework, BGA will increase in popularity.

Plastic ball grid array (PBGA) is made of high temperature PCB laminate. As in CBGA, the internal connection is made either with wire bond or by flip-chip interconnection. (See Figure 15-1.) For higher thermal performance, a heat slug can be incorporated inside the package. The solder balls are 0.8 mm diameter eutectic 63% Sn, 37% Pb balls (melting point 183°C) or 62%Sn, 36% Pb and 2% Ag balls (melting point 179°C).

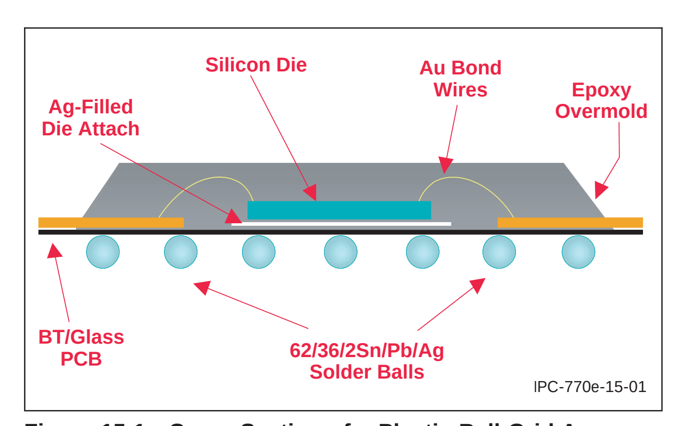


Figure 15-1 Cross-Section of a Plastic Ball Grid Array (PBGA) Package

The resins used in PBGAs have T_g (glass transition temperature) necessary for high temperature stability. BT (bismaleimide triazene) resin is the most commonly used resin for PBGA. Driclad, another resin material developed and patented by IBM, is also used for PBGAs. These materials have CTE very similar to that of commonly used FR-4 laminate (16-20 ppm) and hence do not pose any solder joint reliability concerns. Driclad is more resistant to moisture but all PBGA packages are considered to be extremely moisture sensitive. Hence all PBGA packages are susceptible to the popcorn effect (like any plastic package). The failure is generally seen as a crack in the package or delamination in the die-attach region.

The PCB layer in the package can be two-layer or multilayer depending upon package complexity. The ball attachment process is as follows. Liquid flux is dispensed on a strip containing multiple packages after they have gone through wire bonding and plastic molding process steps. Then balls of the desired size (as shown in Table 16-4) are placed either by gang placement machines or dispensed en mass with a stencil-like fixture. The flux holds the balls in place during reflow in an inert (nitrogen) environment. N_2 helps provide consistent ball quality and keeps them from oxidizing during reflow. However, N_2 is not necessary for final reflow of the package to the PCB. The eutectic solder balls provide ‘‘controlled collapse’’ and self-alignment during reflow, compensating for some misplacement.

PBGA is generally a low-cost and low profile package. However, in some cases, PBGA packages may cost more than fine-pitch packages. The reason is that expensive fine-line boards and high temperature resins are used in PBGAs. Also, BGA is a relatively newer technology. With time, the cost differential between PBGA and fine-pitch should disappear. This has been the case between through-hole and standard surface-mount packages.

There are some major issues with the plastic BGA package. In addition to being extremely moisture sensitive, it is difficult to rework. The PBGA balls are difficult to reball after they collapse during rework. The high melting point CBGA balls, on the other hand, do not melt during rework.

The PBGA package is susceptible to warpage. The edges of the package tend to lift up, causing no connection on the outer rows. As expected, the larger PBGA packages are more susceptible to warpage than the smaller packages. This is one of the reasons why many believe that the lead coplanarity allowed should be 150 µm (in most other components it is 100 µm). Warpage is less of an issue if solder paste (as opposed to flux only) is applied for reflow. The package warpage is caused by CTE mismatch between the PBGA substrate and the silicon inside. This problem becomes serious if the die is large.

Unlike CBGA, CTE mismatch does not exist between the PBGA package and FR-4 PCB. However, CTE mismatch between a large die and package body can cause solder joints near the corner of the die to crack. Solder balls beneath the corner of the chip generally fail first. However, if balls are depopulated under the die, the corner joints fail first as in CBGA.

15.2.2 Ceramic Ball Grid Arrays (CBGA) The Ceramic BGA (CBGA) is also called SBC (solder ball connection) by IBM. Figure 15-2 shows an illustration of a CBGA. The internal connection in the package can be either with conventional wire bonding or by flip-chip. Figure 15-2 shows

flip-chip bonding inside the package. The package can be either cavity up or cavity down as in the LCCC discussed earlier. The solder balls are high temperature solder (90% lead and 10% tin) with a melting point of 302°C. The balls are attached to the package with eutectic solder (63% Sn, 37% Pb). The ball diameter is 0.8 µm. The body size of CBGA is from 18 to 32 mm.

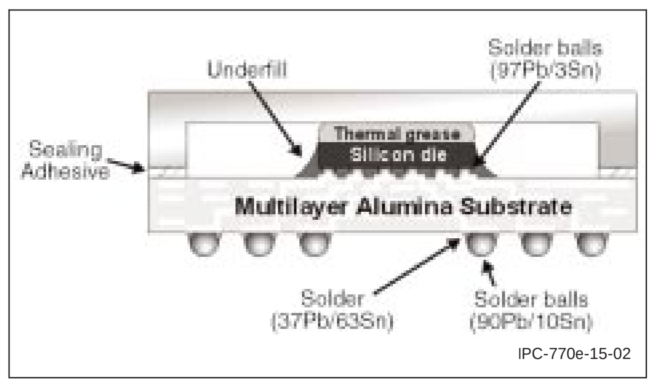


Figure 15-2 Cross-Section of a Ceramic Ball Grid Array (CBGA) Package

The CBGAs are hermetic (do not absorb moisture) and hence are not subject to the popcorn effect like PBGAs. Also, since the solder balls have a high melting point, they do not melt during rework and, unlike PBGAs, can be reballed for reuse. The balls are 1.25 mm in diameter and provide sufficient standoff for reliability and cleaning.

The disadvantage of CBGA is that its high thermal mass makes reflow profile development difficult. Also, like the LCCCs discussed earlier, the CTE mismatch between the package and the board limits useful life. Studies have found that the corner joint (farthest distance from neutral point or DNP) fails first. The failure occurs between the ball and the board land. The CCGAs, on the other hand, generally fail in the columns.

15.2.3 Ceramic Column Grid Arrays (CCGA) Ceramic column grid array, shown in Figure 15-3, is used for larger packages (32 to 45 mm). Like CBGAs, and PBGAs, they also use multilayer ceramic packages. They are very much like PGAs but with lower pitch and more fragile leads (columns).

The CCGA column diameter is about 0.5 mm and the column height varies from 1.25 to 2.0 mm. These columns are attached to the package either by eutectic (63Sn/37Pb) solder or they are cast in place using 90% Pb and 10% Sn.

Taller columns increase solder joint reliability by taking up strains created by the CTE mismatch between the package and the board. Studies have found that CCGAs can be three to five times more reliable than CBGA.

Longer columns reduce electrical performance and increase the overall package profile. Also the columns are not as rugged as solder balls and are susceptible to handling damage like fine pitch.

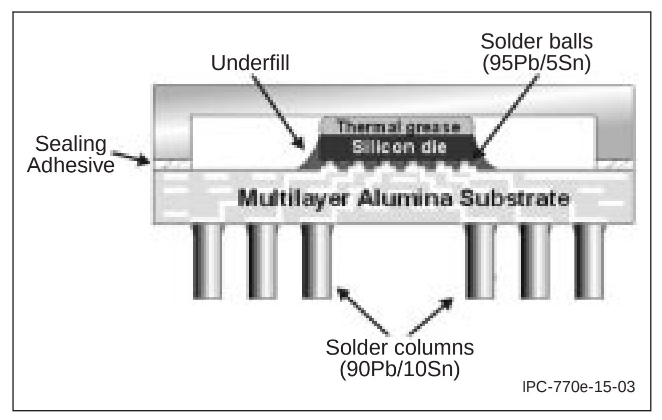


Figure 15-3 Cross-Section of a Ceramic Column Grid Array (CCGA) Package

15.2.4 Tape Ball Grid Arrays (TBGA) Tape ball grid array (TBGA), shown in Figure 15-4, is another low cost low profile package. It uses a low dielectric substrate (polyimide) and a two-metal layer TAB-type substrate (1 signal & 1 ground). In TBGA, the CTE mismatch issues are nonexistent since adhesive and flexible substrates take up strains. IBM reported no failures in 0-100°C thermal cycling or 22,000 power cycles (25-75C, 3W). TBGAs can use flip-chip or TAB interconnection to make a lower die pitch more possible than with wire bond. For example, in wire bond the pitch is generally 100 µm but with TAB used for TBGA, the pitch can be 75 µm. The use of smaller pitch helps in shrinking the die.

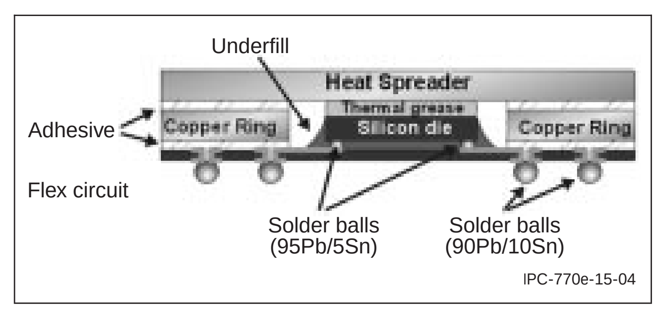


Figure 15-4 Cross-Section of a Tape Ball Grid Array (TBGA) Package

Unlike CBGA, there is no eutectic solder joining the package to the balls. Partially melting the 0.65 mm diameter balls, 90% Pb, 10% Sn, attaches them to the lands. Commonly, the TBGA pitch is kept at 1.25 mm centers and their body sizes vary from 21 to 40 mm.

One concern with TBGA is that it allows only a single wiring plane in the substrate. Thus, TBGA is essentially restricted to being a single-chip package. The other types of BGAs discussed above can accommodate multiple dice because they use multilayer substrates (either ceramic or BT resin substrates). TBGA also requires a gold bumped die that may not be available in the open market. TBGA is also a moisture sensitive package since polyimide absorbs moisture.

15.3 BGA Connectors

15.3.1 Assembly Considerations for BGA Connectors Several items need to be addressed concerning the placement and soldering of BGA connectors to a PCB substrate.

Some BGA connector designs do not lend themselves to a vacuum pick-up using standard SMT nozzles. In this case, two options are available:

- Using a custom nozzle for mechanical chuck pick-up.
- Designing the BGA connector with a cap or other temporary surface so a standard vacuum nozzle can be used.

Both options can be successful in production, and the best option is highly dependent upon the connector design. Figure 15-5 shows a top and bottom view of a high pin, BGA connector that requires a special pick-up tool.

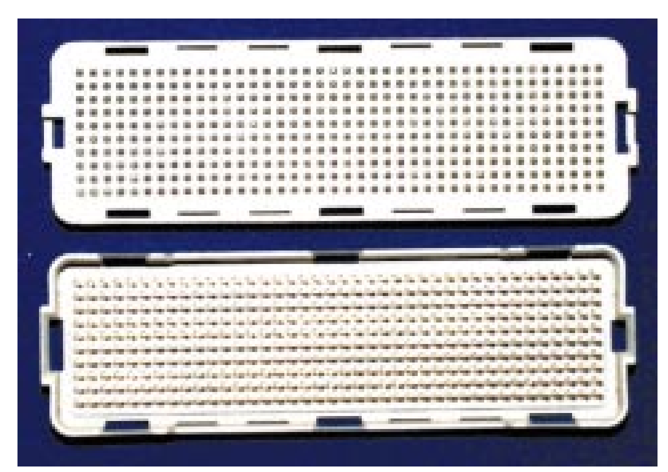


Figure 15-5 BGA Connector

Depending on the connector material, reflow profiles have to be examined and compared to the T_g temperature of the connector material. When the temperature of the connector increases beyond the T_g point, the connector tends to either bow toward the board (''flatten out'') or bow away from the board (''warp''). The actual behavior is a function of the connector geometry, connector material and the surface tension of the connector balls to the substrate.

Also included in this analysis are the connector coplanarity requirements for successful soldering. The material properties (behavior during reflow) and the overall connector size dictates the connector ball coplanarity requirements. Typically, BGA connector's coplanarity requirements are stricter than standard BGA components due to their increased size.

15.3.2 Material Considerations for BGA Connectors During the life of the product, the circuit board assembly undergoes many varying thermal cycles. These thermal cycles cause material expansion and contraction to the assembly components, including the BGA connector. Therefore, material selection for BGA connectors is significant due to the thermal interaction of the connector to the PCB substrate.

Specifically, the BGA connector material's coefficient of thermal expansion (CTE), must be matched to the CTE of the PCB substrate material. This is not typically a problem on gull-wing connectors due to the construction of the lead to the connector body and the solder joint formation of gull-wing joints vs. BGA joints.

If there is a significant CTE difference between the BGA connector (typically a LCP material) and the PCB substrate (typically FR-4), the resulting thermal stresses on the solder joints could cause cracking and ultimately solder joint failure.

15.4 Components Package Drawings This section discusses material specific to plastic packages that have been registered under JEDEC. While some suppliers offer ceramic LGA packages, they are not yet registered with the EIA. Figure 13-4 from the JEDEC JC-11 registration documentation contains package outline drawings for plastic BGAs. The body sizes are ''hard metric'' and apply to square bodies with symmetrical array.

The area array package is typically smaller, pin for pin, than the leaded alternatives. In addition, the ball contact is not easily damaged during the assembly processes. Both BGA and fine pitch BGA devices allow for depopulation of contacts to meet specific I/O requirements; however, the grid location conventions must be observed. Because of the higher lead density on the BGA and fine pitch BGA component families, assembly specialists have found that both printed board quality and surface finish directly affect the overall manufacturing process yields.

15.5 Component Procurement

15.5.1 Shipping Media ESD Sensitive components must be shipped in ESD-approved static dissipative containers and packing materials.

15.5.2 Delivery System

15.6 Handling and Storage Surface mount grid array components should be stored in containers that prevent damage to the I/O contacts. ESD precautions must be taken during the handling of components while loading trays, feeders, etc.

15.6.1 ESD Protection Components sensitive to electrostatic discharge must be handled in accordance with EIA-625 or an equivalent ESD program.

15.6.2 Moisture They are currently a Class 3 component and require special handling. They must be used within 24 hours of their removal from dry pack and must be stored in low humidity once opened (see J-STD-020).

16 MOUNTING STRUCTURE REQUIREMENTS HIGH PIN COUNT AREA ARRAY

16.1 Characterization and Classes - Interconnecting Structures (Printed Boards) The printed board design is very similar to the standard surface mount design. Surface mount lands (pads) are positioned in an array that duplicates the array found on the BGA package. The PB footprint shall have circular lands matching each termination on the BGA. The diameter of the PB land should be approximately the same as the land on BGA. Since the array pattern on the board is much more dense than standard surface mount designs, multilayer technology is typically required.

The surface mount land-to-via connection can be accomplished by several ways. The first, and most often used, is the dog-bone approach. This design has the via offset from the land which is connected with a small trace. The trace is considerably smaller than both the land and via that results in a dog bone shape.

Another approach is Via-In-Pad (VIP) technology. This design may utilize:

• Resin-filled via which is over-plated with copper.

• Via plugged hole.

• Mechanically-drilled blind via.

• Microvia (photo, plasma, laser, defined etc.).

16.2 Standardization Standardization of BGAs considers variations that exist in determining land patterns. These include the diameter of the individual ball; the positional accuracy of the ball in relationship to a true position on the component and the board; and the manufacturing allowance that can be held for the land on the substrate that mount the particular ball.

The land pattern of the component (where the ball is attached) and the land pattern of the substrate mounting structure (printed board) should be as similar as possible. Component manufacturers have made their determinations that the land pattern of pad on the component should be less than the ball diameter. They base their conclusions on the resulting nominal ball diameter with a slight reduction in the land approximation.

16.3 Ball Pitch Ball Grid Arrays are divided into two groups of pitches. The first group is regular which is 1.50, 1.27, and 1.00 mm. The second group is the fine pitch, which has the following pitches 0.80, 0.75, 0.65, 0.50, 0.30 and 0.25 mm. The present usage shows that 1.27 mm as being the most popular followed by the 0.80, 1.00, 0.75, and 0.50 mm. At the moment, very few component manufacturers are providing parts with 1.5 mm pitch, as the pressure is on form factor in order to keep BGAs as small as possible. Pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 16-1 shows the characteristics of those balls that are used with pitches of 1.5 mm through 0.5 mm.

Table 16-1 Ball Diameter Sizes

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.75	0.90 - 0.65	1.5, 1.27
0.60	0.70 - 0.50	1.0
0.50	0.55 - 0.45	1.0, 0.8
0.45	0.50 - 0.40	1.0, 0.8, 0.75
0.40	0.45 - 0.35	0.80, 0.75, 0.65
0.30	0.35 - 0.25	0.8, 0.75, 0.65, 0.50

16.4 Future Ball Conditions Although not required for the BGAs shown in Table 16-1, future ball sizes contemplated are shown in Table 16-2.

Table 16-2 Future Ball Size Diameters

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.25	0.28 - 0.22	0.40
0.20	0.22 - 0.18	0.30
0.15	0.17 - 0.13	0.25

16.5 Land Approximation In each instance, component manufacturers and board designers are encouraged to reduce the land size by some percentage of the nominal ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined to be 0.1 mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC). Table 16-3 shows the reduction characteristics, the nominal land size, and the target land dimensions.

Table 16-3 Land Size Approximation

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25%	0.55	0.60 - 0.50
0.60	25%	0.45	0.50 - 0.40
0.50	20%	0.40	0.45 - 0.35
0.45	20%	0.35	0.40 - 0.30
0.40	20%	0.30	0.35 - 0.25
0.30	20%	0.25	0.25 - 0.20

The information shown in Table 16 provides data on land patterns and their variation to accommodate four ball diameters. Many component manufacturers use solder resist-defined lands (see Section 1, 6.2.2). When this technique is employed, the nominal land diameter should be increased

by the amount of solder resist encroachment on the land (usually about 0.1 mm). The opening in the solder resist window then represents the diameter to which the ball becomes attached, while the actual land is slightly larger to accommodate the solder resist-defined land concepts. Routing density is now decreased, since the land is larger.

Table 16-4 shows future land size approximations. These indications are for ball sizes from 0.25 mm to 0.15 mm.

Table 16-4 Future Land Size Approximations

Nominal Ball Sizes (mm)	Reduction	Nominal Land Size (mm)	Land Variation (mm)
0.25	20%	0.20	0.20 - 0.17
0.20	20%	0.15	0.15 - 0.12
0.15	20%	0.10	0.10 - 0.08

16.6 Physical Conditions The high pin count area array device family includes square and rectangular package configuration and is furnished in plastic, metal or ceramic base materials. The base material serves as a mounting structure for attaching the die.

Depending on the physical characteristics of the base material, wire bond or direct chip attach technologies may be employed for die attachment.

17 ASSEMBLY HIERARCHY HIGH PIN COUNT AREA ARRAY

17.1 Process Steps BGA assembly has been proven to be consistent with the best current practices (BCP) for surface mount (SM) assembly. They can be assembled concurrently with peripheral leaded devices on a typical automated assembly line. Paste is printed, packages are placed and then the boards are reflowed. Reflow is typically done in an IR/Convection or forced air convection oven with a profile similar to those used for SM assembly. The assembly process of the BGA is robust because the package tends to self-center during reflow and the molten solder ball can accommodate to board or package planarity variations. Packages are available in trays or tape and reel and can be placed with standard placement machinery without special considerations.

17.1.1 Sequence The following are typical process steps for a Type 1 assembly:

1. Apply solder paste.
2. Verify solder paste.
3. Place surface mount components.
4. Verify placement.
5. Solder reflow.
6. Verify reflow.
7. Clean if required.

17.2 Process Step Analysis There are several available paths to utilizing BGA effectively. The length of each path depends on what design and assembly facilities a company presently has, and how quickly they can be made ready for production.

1. Select a list of candidate products for BGA.
2. Develop an equipment list based on the projected volume needs. If sufficient in-house expertise does not exist, it may be desirable to use a reputable training center or consultant to save cost and time.
3. Organize a team representing design, production, test, quality, and purchasing. This team is responsible for component and equipment selections and review.
4. Develop a comprehensive BGA design guide that stresses manufacturability using existing standards where possible.
5. Design the candidate products starting with the conversions of existing products using fine pitch components.
6. Conduct rigorous assembly and test reviews. Carefully monitor component purchasing to assure that components have the specified package, shipping method, metallization, solderability, and orientation in the shipping containers.
7. Develop comprehensive workmanship standards and a process control system that is statistically sound.
8. Design the remaining candidate products.

17.3 Attachment Issues The interconnections between the package and the substrate (Board structure) is typically made with a solder pillar connecting the lands on the bottom of the package and a set of matching lands on the substrate. There are two common ways of forming the solder pillars:

In Ball Grid Arrays (BGAs), a solder ball is fused to the pads on the bottom of the package during package manufacture. In assembly, the solder balls are reflow soldered to the substrate lands (with the assistance of flux or solder paste). Since the solder ball or paste becomes molten during reflow, the package has a tendency to self-center on the footprint producing a very robust assembly process. The solder ball volume and the weight of the package determine the height of the solder pillar.

In Column Grid Arrays (CGAs), the solder pillars are cast directly onto the package lands out of high melting point solder. They are soldered to the substrate footprint with solder paste so that only the very bottom and the pillars reflow. This provides a controlled height of the solder column (with an accompanying increase in fatigue lifetime) at the cost of a less robust assembly procedure. CGAs are most common in ceramic body packages.

17.4 Reflow Reflow is typically done in an IR/convection or forced air convection oven. Solder paste should be applied using a stencil having an aperture of no greater than the pad diameter on all lands. The stencil thickness should be no less than 6 mils. For plastic components, the assembly process is relatively insensitive to solder paste thickness as long as planarity is good enough for the solder paste to make contact with both package and land. For the relatively heavier ceramic devices with eutectic or near eutectic solder balls, thick solder paste deposits may result in solder bridges as the weight of the package causes the solder balls to collapse during reflow.

17.5 Preclad When the lands are precoated with a defined amount of solder, a tacky solder flux is applied to the board before component placement.

18 COMPONENT CHARACTERISTICS FLIP CHIP DIRECT CHIP ATTACH

18.1 Types of Flip Chip Joints

18.1.1 Solder Bumps The solder bump forms the electrical and mechanical bridge between the chip and next level assembly. It absorbs the strain between the chip and next level of assembly caused by variations in their relative thermal expansion rates.

The solder composition of the flip chip bumps varies according to required mechanical and thermal properties. Common bump compositions include:

- 97 PbSn
- 95 PbSn
- 90 PbSn
- 63 SnPb
- 50 InPb

18.1.2 Nonsolder Type Bumps

- Ni/Au bump
- Cu ball
- Au bump
- Conductive polymer bumps

18.2 Characterization and Classes of Flip Chip Joints

18.2.1 Meltable Solder Joints A common meltable solder joint is the Controlled Collapse Chip Connection (C4) type solder bump. IBM developed this interconnect technology during the 1960s as an alternative to manual wire bonding. Often called ‘‘flip chip,’’ C4 attaches a chip with the circuitry facing the substrate. C4 most commonly uses solder bumps deposited through a metal or polymer mask onto wettable chip pads that connect to matching wettable substrate pads. Flipped chips are aligned to corresponding substrate metal patterns and interconnections that are formed by reflowing the solder bumps, thereby simultaneously forming the electrical and mechanical connections. Figure 18-1 is an example of a typical meltable solder bump.

Another type of meltable solder joint is the electrodeposition solder bump. It offers a wider range of SnPb composition than evaporation, and thus offers greater control over mechanical and thermal properties. Electrodeposition can produce very small diameter bumps.

A third type is the printed solder bump. It offers compositions of very tight control of solder paste compositions and offers a wide selection of different solder types.

Examples: High Pb based PbSn, PbIn, SnPb Eutectic and Indium-based solder joints.

18.2.2 Partially Meltable Bumps In this class of solder joints, the bump metallurgy remains partially nonmelting during the joining operation.

Figure 18-2 is an example of a typical partially meltable Solder Bump.

Examples of positive standoff bumps include Cu stud with eutectic solder tip or high Pb stud-tipped with meltable SnPb eutectic, etc.

18.2.3 Nonmelting Bumps In this class of interconnects, a positive, nonmelting standoff is formed that can be soldered or adhesive bonded to the next level of packaging. Figure 18-3 is an example of a nonmelting bump.

Examples: Cu ball standoff, Ni/Au bump, Au Bump, Stud ball bumping.

Stud ball bumping is a variant of traditional wire-bonding in which the ball is formed on the bond pad and the wire is broken off to leave a short tail. The tail is then flattened or coined to create uniform bump height. Bumps can be made from gold or solder wire. They cannot be used over active circuitry.

18.2.4 Polymeric/Conductive Adhesive Bumps There are several types of polymeric conductive bumps. The isotropic conductive paste is one high volume bump technology. Conductive adhesive is used in two bump technologies (or is it that there are two types of conductive adhesives used in bump technology?). One is isotropic conductive adhesive where current conducts in all directions. The other is an anisotropic conductive adhesive where the current conducts only in concentrated particle areas. Figure 18-4 is an example of an isotropic conductive adhesive bump.

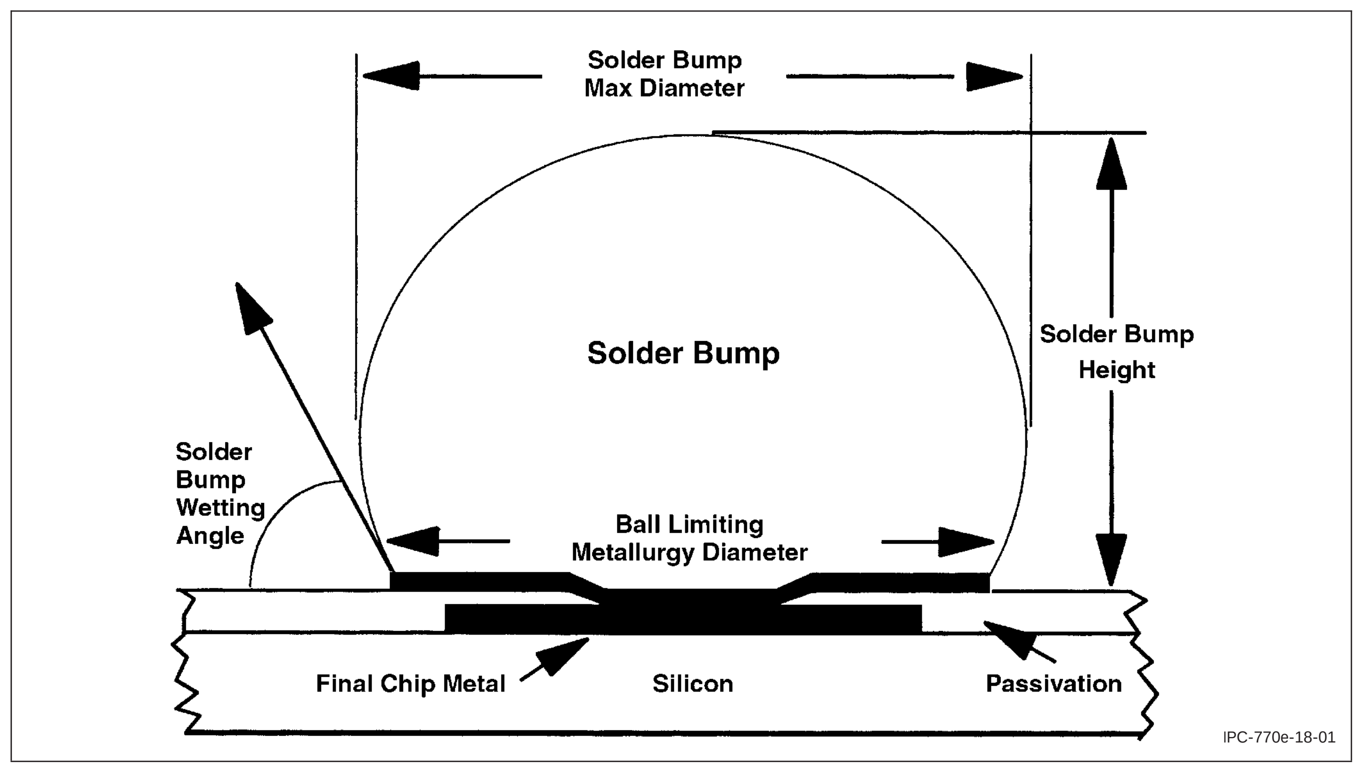


Figure 18-1 Typical Meltable Solder Bump

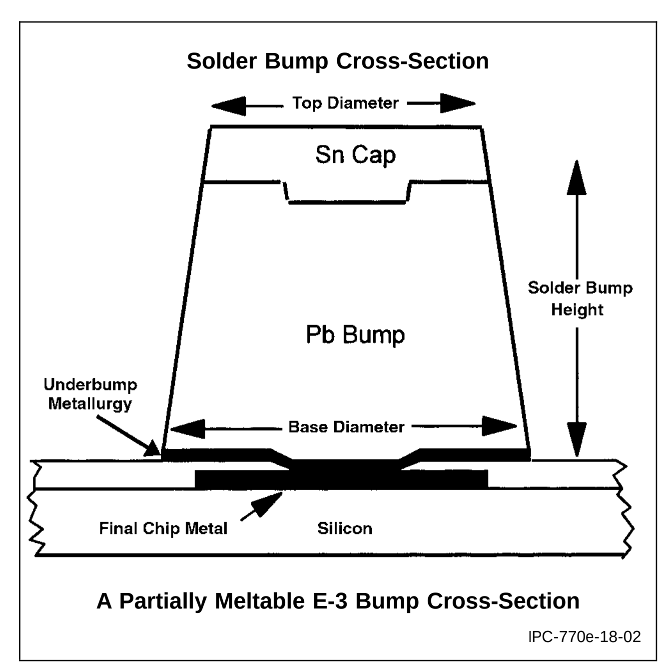


Figure 18-2 Partially Meltable Solder Bump

Examples: Ag, Au, or Cu filled epoxy, Ni particle filled epoxy, plated polymer balls in adhesive, Ag filled thermoplastics, Au plated Ni particles, etc.

18.2.4.1 Conductive Paste Method Conductive paste methods have been implemented in mass production.

In one method, the LSI driver chips are plated to form 50 µm copper bumps with a thin overcoat of Au. Then either the bumps or panel electrode are coated with the Pd-Ag

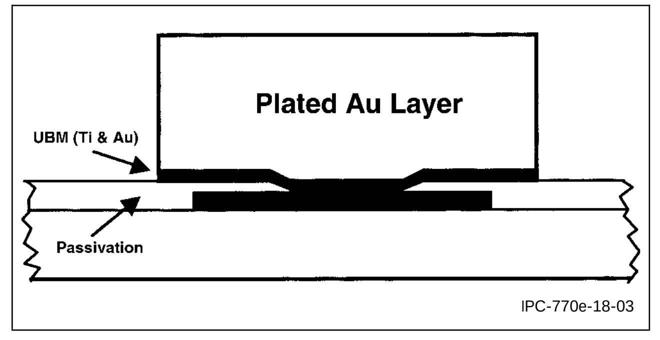


Figure 18-3 Nonmeltable Bump

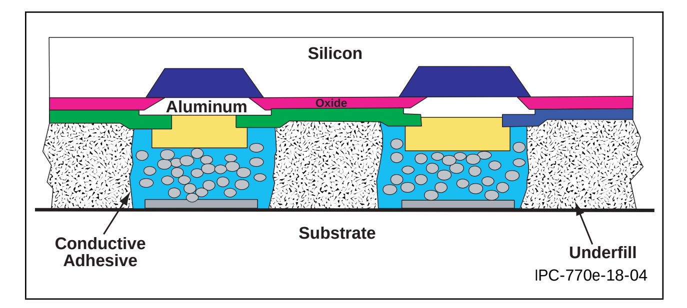


Figure 18-4 Isotropic Adhesive Bump

paste. Next, the coated bumps are aligned with the panel to electrodes and joined under pressure. Setting the paste and coating the chip with a protective resin follows.

Isotropic conductive bumps are typically 40-60 microns in height, depending on stencil thickness. The minimum bump size is 50 micron diameter and the pitch is 4.0 mil. The height of the bump can be increased for use with PCB

laminates with solder resists. Contact resistance of isotropic conductive bumps is typically 10-15 milliohms.

18.2.4.2 Conductive Adhesives Process Screened-on conductive epoxies are available, but their reliability is yet to be proven. The conductive material is usually gold or some other oxidation-resistant metal. Part of the function of the conductive filler, due to the sharp or angular particles, is to pierce through the native oxide formed on the In/Sn oxide during bonding.

Other flip-chip technology requires Under Bump Metallurgy (UBM), such as electroless Ni/Au or Au plating. The isotropic conductive polymers can be epoxies, B-stage epoxies or thermoplastics.

Conductive particles dispersed into insulating adhesive provide an interconnect wedge between pads or posts on the chip-to-lands interconnection structure. There are two types of adhesives:

- Isotropic conductive adhesives in which current is conducted in all directions by the particle-to-particle contacts.
- Anisotropic conductive adhesives containing a concentration of particles too low to conduct electricity in any direction.

During the assembly process, excess adhesive is squeezed out between the pads on the chip and the substrate leaving single particles to bridge the chip substrate gap. The gap is established by the diameter of the conductive particle. The advent of flat panel displays has greatly accelerated the use of these techniques. Anisotropic adhesives eliminate the need for underfill, however the planarity requirements are stringent.

18.3 Component Design for Circuit Boards When the die or component is in the design stage, the assembler and circuit board designer must have inputs in pad/bump layout to ensure the die or component does not violate circuit board design rules; (see J-STD-012, J-STD-026 and IPC-2225).

18.3.1 Design Considerations (repeated information) In this methodology, the chip is attached to circuitry facing the substrate. Solder bumps are deposited onto a wettable chip pad that connects to matching wettable substrate lands as shown in Figure 18-5.

Flip chips are aligned to corresponding substrate metal patterns. Reflowing the solder bumps forms the interconnections. The simultaneous forming of the electrical and mechanical connections is shown in Figure 18-6. The joining process is self-aligning, i.e.; the wetting action of the solder aligns the chip-bumped pattern to the corresponding substrate lands. This action compensates for chip-to-substrate misalignment incurred during chip placement. An added feature of the flip-chip process is the potential to rework. Several techniques exist that allow the removal and replacement of chips without scrapping the chip or substrate. Depending on substrate material, rework can be performed numerous times without degrading the quality or reliability provided that the mounting substrate can tolerate the rework temperatures. Injection of chip underfill, as illustrated in Figure 18-7, improves reliability most notably in cases of high thermal expansion mismatches. Currently, any injection must be performed prior to the application of chip underfill.

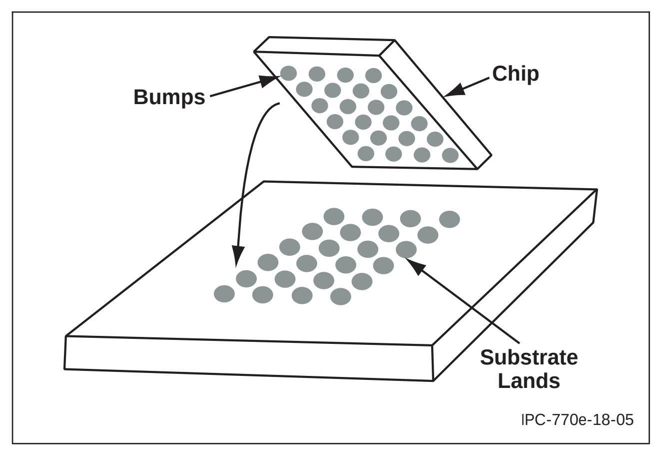


Figure 18-5 Flip Chip Connection

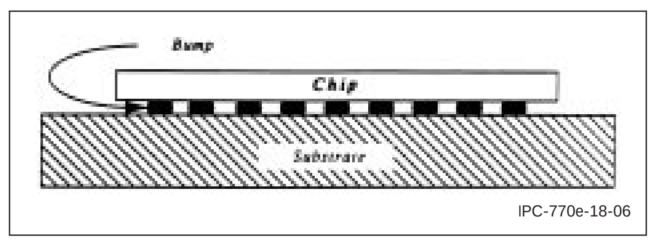


Figure 18-6 Mechanical and Electrical Connections

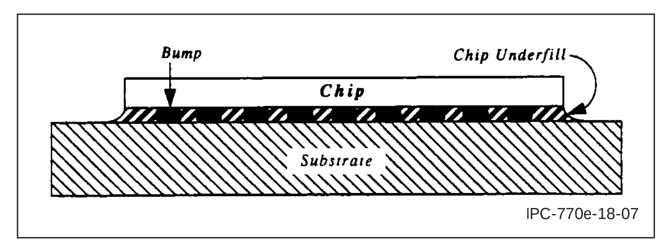


Figure 18-7 Joined Chip with Chip Underfill

An alternate joining technology to reflowable bump flip chip is one that has low melting solder bumps attached directly to a printed board. The bump on the semiconductor die is not reflowed, instead the lower melting solder on the printed board wets the bump on the die to form the interconnect.

18.3.2 Chip Size Standardization Standardizing the size of semiconductor chips may appear to be counter to the objectives of the chip designer and supplier. Many chip suppliers rely on the ability to shrink the size of a chip as

it matures. This results in more good chips per wafer. This strategy is sound if the chip is the dominant cost item for the product. Today many products are dominated by packaging, as opposed to chip cost. Prime examples are discrete diodes and transistors. These are low lead count logic devices and general-purpose analog chips. These products benefit from the cost reduction and performance improvements possible with chip scale packaging.

Chip suppliers and their customers benefit if when converting their die-to-chip scale packages they adhere to area size standards. The EIA/JEDEC JC-11 Committee establishes these standards. The committee develops standards for outlines of semiconductor devices as their counterpart in the EIA Committee develops standards for passives. Accepting chip size standards reduces the need for many different tape stocks for the tape and reel packaging of these devices. Standards also provide users with multiple sources for the same device.

18.3.3 Bump Site Standards The chip scale bump grid array packages give chip designers significant freedom to choose the bump location and the signal type transmitted on the bump. Chip suppliers should observe standards for grid pitch, bump size and bump location. Optical assemblers use placement machines that place the package based on the edge dimensions. This is because the machine cannot see the bump locations. The placement accuracy and assembly yield depends on the assumed location of the bumps relative to the distance from the edge of the package and the bump grid.

18.3.4 Peripheral Lead Standards The lead pitch standards for peripheral leaded chip scale packages, should follow the existing standards set by the JEDEC JC-11 Committee. Applicable pitch standards are 0.2 mm, 0.3 mm, 0.4 mm, 0.5 mm, 0.63 mm and 0.65 mm. Refer to JEDEC publication JEP-95 for detailed dimensions.

18.3.5 Package Size Standards For the use of package sizes and tolerances, JEDEC JEP-95 is highly recommended. Be sure to refer to the supplier's package drawings in all cases where there may be deviations.

18.3.6 I/O Capability The chip bump process can use most of the chip surface for interconnect pad locations. Some dice have over 2500 bumps on a chip. Chip bumping enables increased interconnect density. Signal, clock and power connections can be placed almost anywhere on the chip. Redundancy means distributions can be optimized for minimum noise and skew, current density and line length. Additionally, on-chip wiring can be reduced since the Z-axis escapes are available where needed. Figure 18-8 compares single row wire bond and bump chips. Each chip is 8 mm square. Wire bond pad size is 76 µm with pads on 100 µm centers. Bump size is 100 µm bumps on a 230 µm center. In this example, interconnect density is increased over 2.4 times using bumping technology.

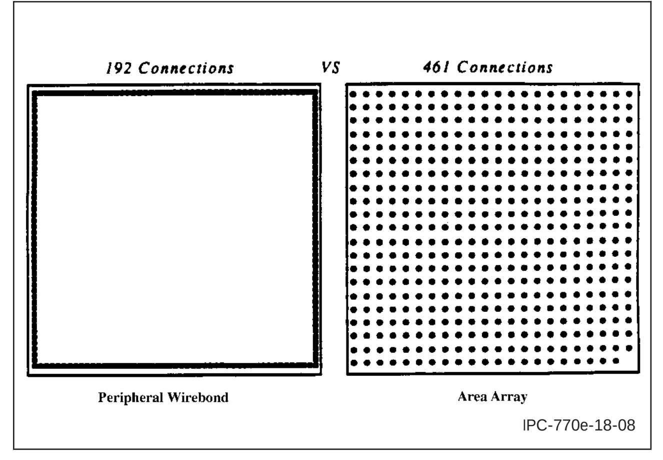


Figure 18-8 Interconnect Density (Peripheral Vs. Area Array)

18.3.7 Alpha Particle Emissions (Soft Errors) Alpha particles may cause soft errors in semiconductor devices. Circuit sensitivity to alpha particle emissions and the allowed soft error rate must be clearly understood for each chip design. Lead contains traces of thorium and daughter elements, e.g., polonium, which emit alpha particles. Circuits resistant to soft errors are designed to withstand alpha particle emission energies. Circuits sensitive to soft errors are DRAMs, closely followed by SRAMs and some flip-flop circuitry. Sensitivity increases as chip geometry shrinks and device (node) critical charge diminishes. The primary concern of the particle emission is the energy that can be imparted to the device circuitry. This is quantified and illustrated in Figure 18-9.

- Alpha Particle = He nucleus = 2 protons + 2 neutrons
- Up to 8.8 MeV of kinetic energy
- Energy converted to electron/hole pairs (3.6 eV per E/H Pair)
- Highest charge density near end of emission track

The resulting effect of an alpha particle can be a distortion of the depletion region's electric field near the alpha particle track as shown in Figure 18-10.

Many materials used in semiconductor packaging emit low levels of alpha particles. This is illustrated in Table 18-1. Emission rates vary for solder and chip underfill depending on the material source. Certain solders may emit a higher rate of alpha particles relative to other materials. These emissions may not be a problem depending on the device circuitry, sensitivity and the allowable soft error rate. If sensitive circuits are present, their proximity to a bump, the

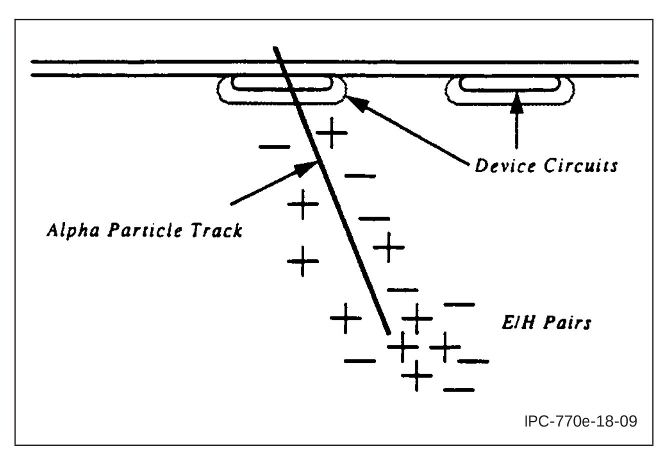


Figure 18-9 Alpha Particle Emission Track and E/H Pairs

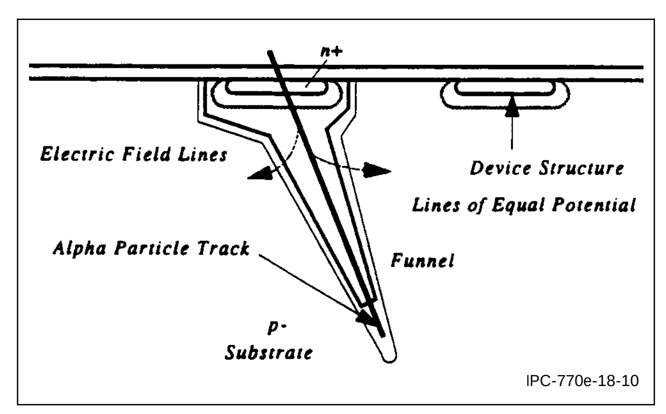


Figure 18-10 Distortion of Depletion by Alpha Particles

bump diameter, the chip structure and the alpha activity rate must be considered in order to estimate the soft error rate. Because distance and materials attenuate alpha particles, emission effects are localized to a bump. Hence, only the bump near the sensitive circuits warrants concern. The total number of bumps on a chip does not necessarily increase or decrease the risk to a sensitive circuit.

Table 18-1 Alpha Particle Emissions of Semiconductor Materials

Materials	Activity [a/(cm^2 - hr)]
High Lead Solder (3/97)	0.05 - 10.0
Alumina	0.1
Chip Underfill (cured)	0.002 - 0.020
Plastic	0.04
Silicon Water	<0.004

18.3.8 Substrate Structure Standard Grid Evolution More recent entries into the arena of substrates designed to meet the demanding requirements of flip-chip and chip-scale technologies appear well suited to the task. These technologies allow for the construction of shortest path routing for the IC device. Typically, based on the concept of standard grids, laminated substrates allow for the production of inexpensive, high performance systems. These technologies are fundamentally elegant in concept and are predicated on the notion that standard grids are required to economically create the most advanced systems in the future.

18.3.8.1 Preferred Grid System On A Printed Board Description positioning connections on a printed circuit board, a grid with a nominal spacing in the two directions of 0.5 mm is to be used.

When a grid with a nominal spacing of 0.5 mm is not adequate, a grid with a nominal spacing in the two directions of 0.05 mm is to be used.

This standard facilitates implementation of common grid systems that are necessary for future high performance systems. Recognized by the IEEE's Computer Society Technical Committee on Packaging, a special task force was appointed in the fall of 1990 to ''seek early consensus on the need to standardize MCM sizes and to propose some possible sizes. The task force recommended 0.5 mm center lines for peripherally leaded packages and PGA standards for area array packages.'' Thus IEC-97 with a base pitch of 0.5 mm with a subdivision of 0.05 mm replaces the familiar 0.100 µm, 0.050 µm, 0.025 µm, and 0.005 µm grid that has been outdated by the wholesale move to metric based measurement systems for electronics. A common grid facilitates common design rules for routing. Table 18-2 illustrates the design rule concept.

An example of a structure that supports the standard grid concept is shown in the Figure 18-11. The use of interposers and substrates allows for the construction of substrates that can offer ''Manhattan routing'' of signals. This eliminates the need for redistribution wiring, which normally consumes large amounts of valuable board real estate while limiting higher performance opportunities. In the illustrated format the interposer joins the inner layers and interconnects them in a single step process. Because the inner

Table 18-2 Design Rules for Substrates for Chip Scale Technology

Feature	0.5 mm Grid (2 lines between pads)	1.0 mm Grid (2 lines between pads)	1.5 mm Grid (2 lines between pads)
Line Width (L)	50 µm [0.002 in]	125 µm [0.005 in]	200 µm [0.008 in]
Space (Line to Line) (S)	75 µm [0.003 in]	175 µm [0.007 in]	300 µm [0.012 in]
Space (Line to Pad) (SC)	50 µm [0.002 in]	125 µm [0.005 in]	200 µm [0.08 in]
Hole Size (H)	125 µm [0.005 in]	200 µm [0.008 in]	250 µm [0.010]
Pad Size (P)	225 µm [0.0009 in]	326 µm [0.013 in]	400 µm [0.026 in]
Wire Routability	40 cm/cm^2 [100 in/in^2]	20 cm/cm^2 [50 in/in^2]	13 cm/cm^2 [33 in/in^2]

layers are thin, the plated through holes have very small aspect ratios for plating and are relatively easy to produce. These inner layers can then be electrically tested before committing them to the finally assembled laminate stack, thus providing greater assurance of a high yield.

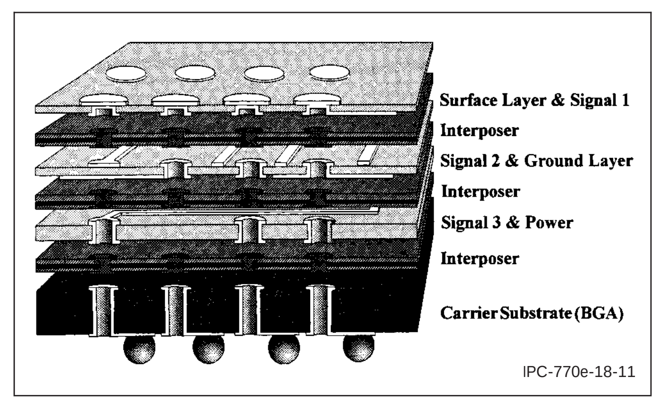


Figure 18-11 Standard Grid Structure

18.3.9 Footprint Design A flip-chip or chip-scale footprint design arranges bumps on the chip surface. When laying out the array of bumps, forethought and planning are required. Bump footprints can be arranged in peripheral, array, or interstitial array formats. Examples of these are shown in Figure 18-12. The size and population of the bumps affects the attachment reliability. The use of the design guide checklist shown in 18.3.10 minimizes reliability problems.

18.3.10 Design Guide Checklist Various design guidelines are applicable in the development of the chip, the CSP, or the attachment process. The guidelines, in some instances, relate directly to the chip manufacturing conditions. In other instances they also apply to chip scale I/Os. In any event, the guidelines are for very specific reasons and designers should consider the following issues:

Guide 1 – Operating temperature must be considered when determining interconnect reliability. Devices with underfill may operate reliably at higher temperature than devices without.

Reason: While solder creep-fatigue is sufficiently characterized for Sn/Pb solders, this is not the case for lead-free solders. Applications require a Design-for-Reliability procedure (see IPC-D-279) and in more complex applications or with the use of lead-free solders evaluation and testing at operating temperatures to determine expected interconnect reliability (see IPC-SM-785 and IPC-9701). The following are the primary thermal and mechanical factors that affect solder joint fatigue:

Range of Temperature Excursion(s)
Time at Temperature Extremes
Component Size
CTE Mismatch
Bump Height
Bump Footprint
Chip Underfill (once underfilled, the performance of the underfill is the key, not the solder)

Guide 2 – Solder and other alpha-emitting materials must be kept an appropriate distance from alpha particle sensitive chip circuitry. For example, a separation of 150 µm is required between C4 bumps (97 PbSn) and sensitive circuitry on polyimide passivated devices.

Reason: Alpha particle emission rate of various materials may be too high for reliable operation of alpha sensitive chip circuitry within close proximity. Measures such as thicker passivations or metal shields can mitigate the effects of proximity.

Guide 3 – Redistribution designs must minimize the inductance and resistance to reduce sensitivity to ESD.

Reason: Increased inductance and resistance of the redistribution line reduces the effectiveness of ESD circuits.

Guide 4 – Maximum current should be modeled for the interconnect system used.

Reason: Current density and therefore reliability, varies with materials, construction, cross-sectional area, operating temperature, etc.

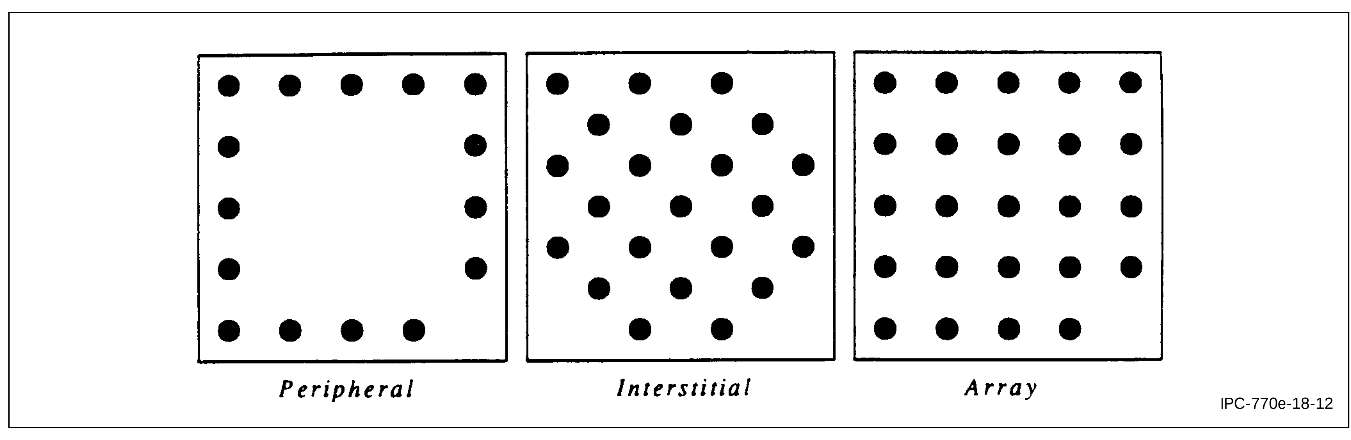


Figure 18-12 Bump Footprint Planning

Guide 5 – Designs should conform to all applicable chip design and wafer fab specifications.

Reason: Design for manufacturability.

Guide 6 – The bump footprint cannot be symmetrical with respect to the X or Y-axis unless there are other features to define orientation.

Reason: Identify chip orientation for subsequent processing.

Guide 7 – At least two bumps are required on each edge of a chip positioned near the chip corner. Dummy bumps can be used to satisfy this requirement.

Reason: Needed for visual inspection and mechanical support of the chip required during joining to maintain parallelism to the substrate.

Guide 8 – Bump diameters are recommended to conform to the mandates of the chosen bump pitch to assure reliable connection without risking shorting between bumps. Some desirable bump sizes are 100, 125, 150 and 250 µm.

Reason: Conforming to individual suppliers' processes and anticipated industry standards (e.g., ANSI, JEDEC, etc.).

Guide 9 – Some minimum number of bumps may be required for manufacturability and reliability.

Reason: To withstand dynamic and steady state mechanical forces.

Guide 10 – In most applications, only one bump diameter per chip/wafer should be used.

Reason: Varying bump diameter may impair chip attachments. Specialized applications for multiple bump sizes per chip/wafer do exist.

Guide 11 – The minimum bump pitch should be held at 250 µm, if possible to facilitate the production of standardized substrates. Multiple minimum pitches cause confusion.

Reason: Minimum pitches prevent bump-to-bump, bump-to-trace and trace-to-trace shorting and provide the distance needed to effectively clean chip joining flux (if applicable).

Guide 12 – Location of bumps near areas requiring visual recognition depends on final bump size as illustrated in Figure 18-13.

Reason: Allows for alignment tolerance such that misaligned bumps do not block or cover areas needed for visual or optical recognition.

Guide 13 – Every bump must be connected to a corresponding substrate metal pad.

Reason: Metallurgical attachment of every bump to both chip and substrate is required for flip-chip interconnect integrity.

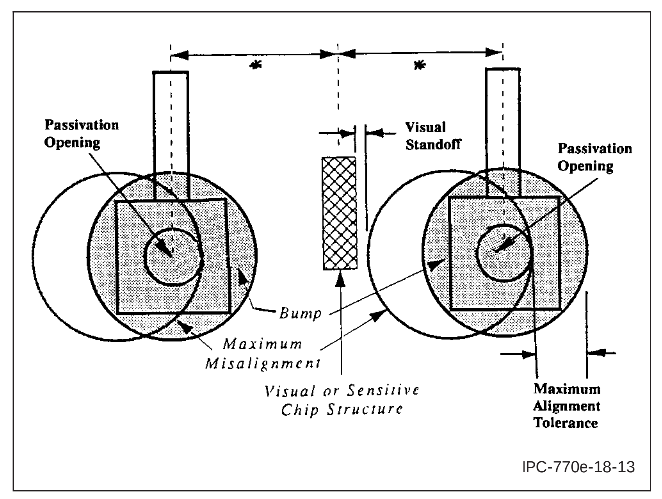


Figure 18-13 Alignment to Visual/Sensitive Chip Structures

18.3.11 Die Design Shrinks Designing a footprint for chips that incur design shrinks requires additional consideration. The approach for this chip design is to locate the critical bumps in the chip's interior. Use outer rows for redundant and mechanical bumps. When the shrink occurs, the outer, less essential rows are lost, but the critical bumps are not affected. As the chip shrinks so does the DNP making the loss of redundant and mechanical bumps less of an issue. This is illustrated in Figure 18-14. With this approach, the bump footprint does not affect the package since the critical connections do not change. Redundant connections to the package simply become open pins. Caution should be exercised when the chip area shrinks so that the bump footprint does not shrink. In addition, provision must be made for orientation and alignment of the shrunk die.

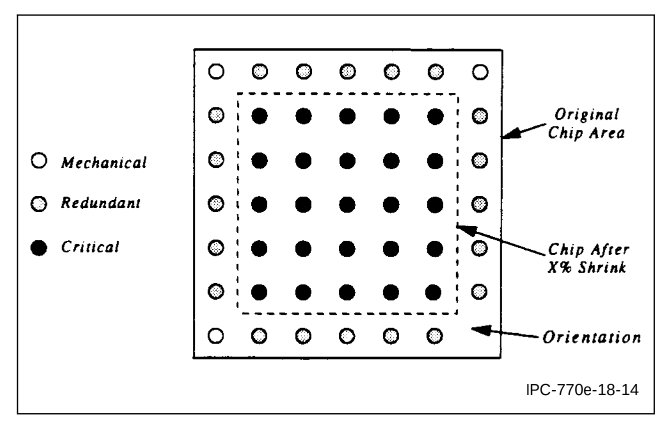


Figure 18-14 Design Shrink Footprint

18.3.12 I/O Drivers on the Periphery Some chip designs require that the I/O drivers are on the periphery with other circuits internal to the chip. Redundant connections for power and signals are desired. When using the approach that positions I/O drivers on the chip periphery, shorter interconnection lengths are always desirable in order to minimize parasitic effects. Bumps should be located as

close to the pertinent circuitry as possible. Figure 18-15 shows redundant power and ground bumps. They are located above the internal circuitry and minimize distribution lengths. Input bumps are placed near the input circuitry and output bumps are placed near output drivers.

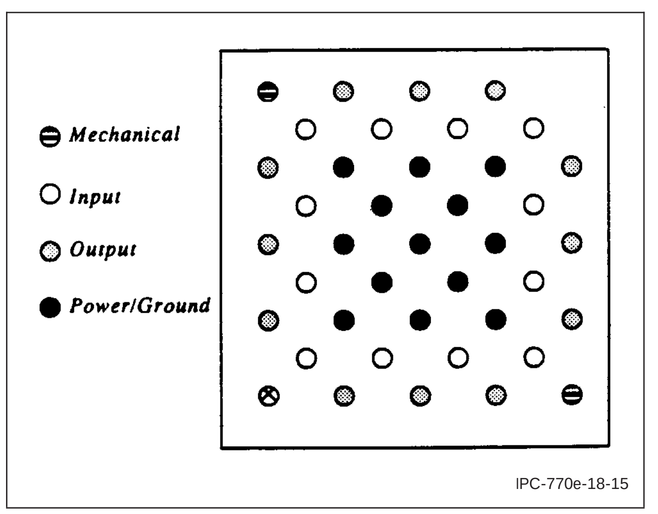


Figure 18-15 Signal and Power Distribution Position

18.3.13 Isolating Sensitive I/Os In some chips, it is important to electrically isolate a sensitive input/output position from crosstalk or other noise. The objective is to surround the area with power and ground bumps as shown in Figure 18-16. Caution should be exercised when placing bumps of different electrical potentials in close proximity, as they could cause shorting problems with dense wafer probes. Bump pitch should be maximized to minimize this hazard.

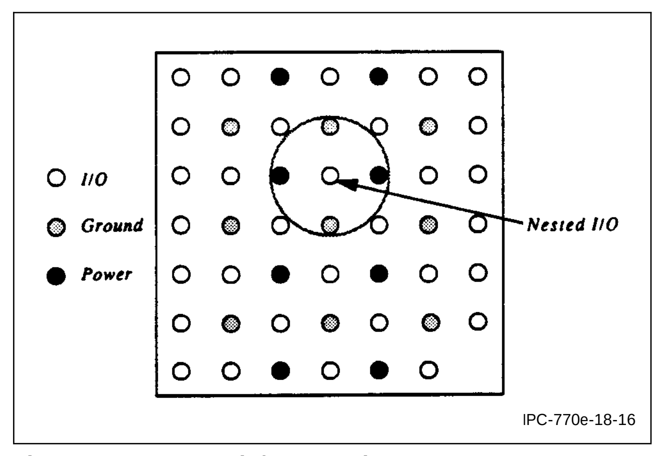


Figure 18-16 Nested I/O Footprints

18.3.14 Printed Board Land Pattern Design The printed board land pattern for flip chips and grid arrays is simply a circle of coated copper whose diameter is the same as the bump's circle. The coating on the copper is one of the common solderability preservatives, such as solder, gold flash, or an organic protective coating (OSP). For MSMT packages, the land pattern may be a solder resist defined opening over the conductive area. A top and cross sectional view of the printed board land pattern is shown in Figures 18-17 and 18-18.

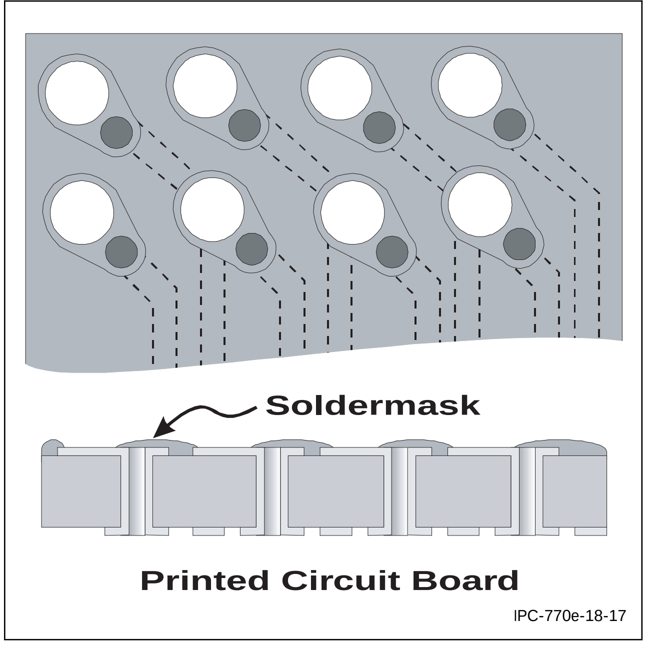


Figure 18-17 Printed Board Flip Chip or Grid Array Land Patterns

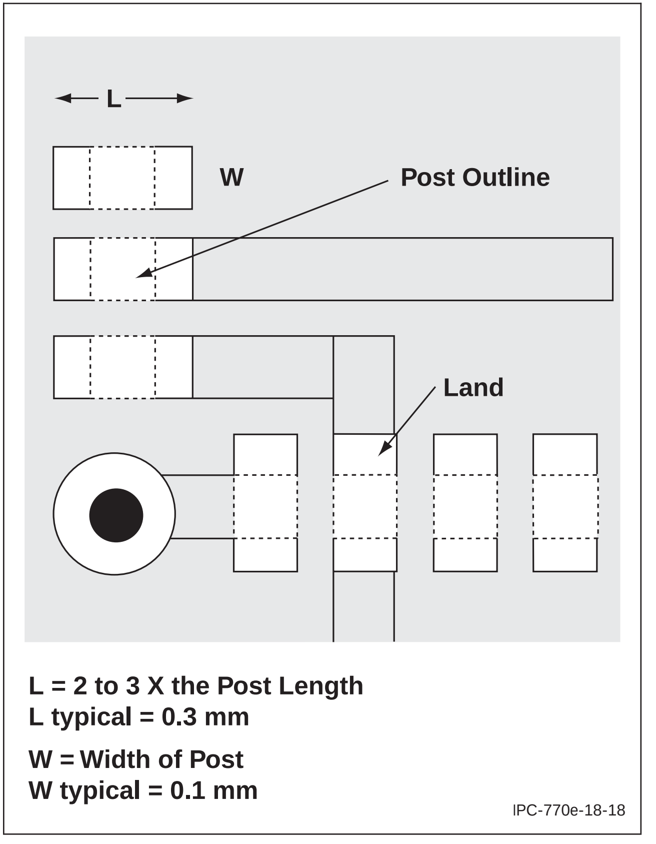


Figure 18-18 MSMT Land Drawing and Dimensions Patterns

18.3.15 High Frequency Performance Because the chip active surface is face down or near the active substrate,

special consideration in trace routing on the chip, interposer, and substrate must be given for flip chips and grid arrays. Changing signal levels on either the chip or the substrate traces close to the chip are coupled. This coupling creates crosstalk, noises, EMF, interference, etc., in the chip or substrate. Controlling the distance, the dielectric between the chip and substrate traces, and characteristic impedance, helps reduce the coupling.

18.3.16 Thermal Design The primary thermal path with bump technologies is through the silicon to the chip backside. To this end, packaging becomes the major component of thermal consideration. Thermal aspects of bump packages provide front and/or backside thermal path. Bump technology offers an added dimension of thermal management. Depending on the application, the designer has the option of selecting the thermal path. The degree of consideration given to thermal design is dependent upon three factors:

- The amount of energy or heat that must be dissipated.
- The desired operating junction temperature of the chip.
- The ambient temperature of the surrounding environment.

Conduction, convection, and radiation are the models for which heat can be dissipated. For bump interconnect, conduction is the primary heat dissipation mode. As illustrated in Figure 18-19, thermal and electrical analyses are analogous.

18.3.16.1 Bump Interconnect Thermal Model The bump thermal interconnect can be modeled as two cylinders between the chip power source and the substrate (see Figure 18-20).

Cylinder 1 represents the inner-layer materials on the chip. Cylinder II represents the pad-limiting metals and the bump size. The heat source is the device in the chip. Because there are three bump interconnect diameter options, cylinder sizes vary accordingly. Assuming that Cylinder I is SiO_2 (k = 1.01 W/mK) and Cylinder II is tin/lead (3/97) solder (k = 36 W/mK) then the approximate interconnect thermal resistance can be calculated for each option (see Table 18-3).

The Cylinder I thermal resistance varies according to the number and specifically, the thickness (L) of inner layers on the chip. As the main contributor to thermal resistance, it should be modeled accurately. Furthermore, interface and bulk resistances have been combined to simplify calculations and illustrations. Bump interconnect thermal resistance for a typical single, double and triple layer metal device are shown in Table 18-4. These values are based on 150 µm bump on silicon where SiO_2 inter-layer dielectric is modeled; (see 17.2 Junction to Case Thermal Models.)

Packaging options can range from hermetic, metallized ceramic modules to printed circuit boards for direct chip or

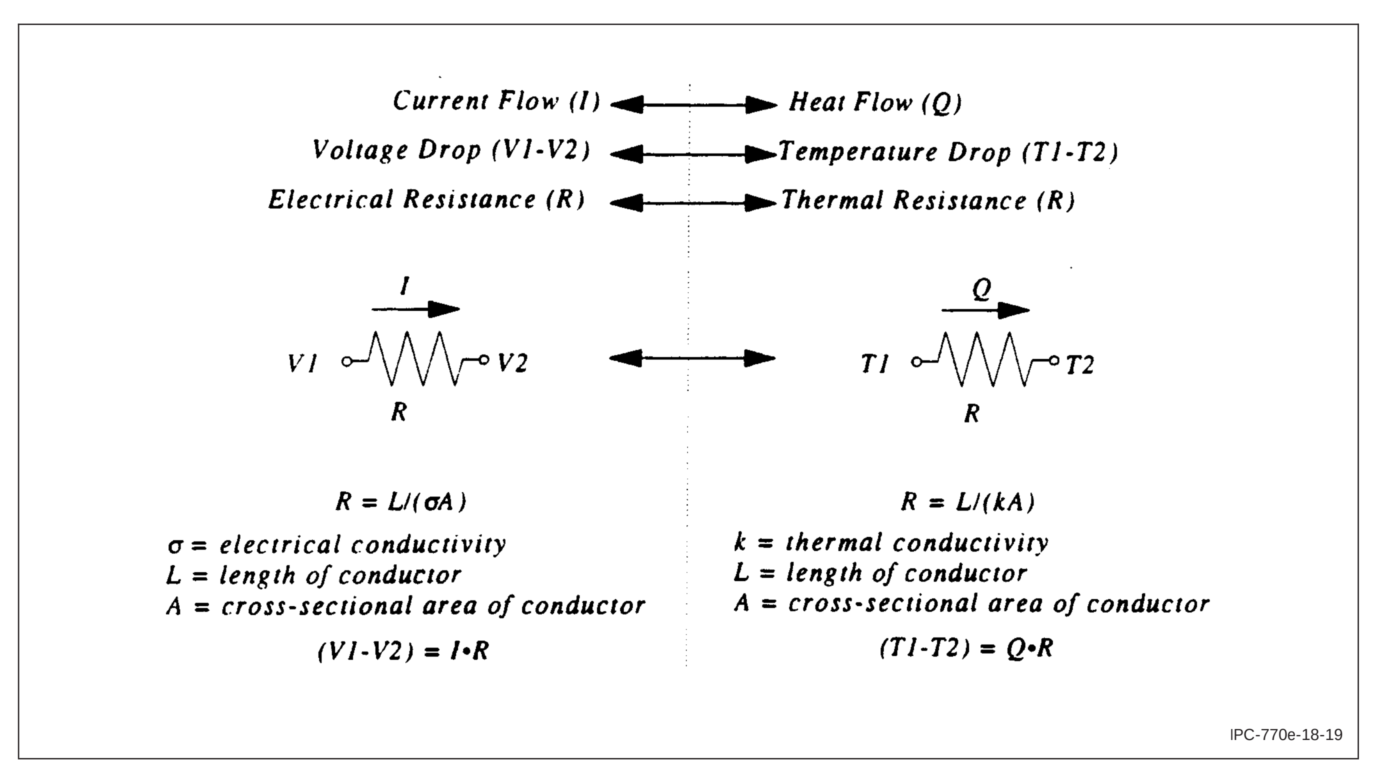


Figure 18-19 Thermal/Electrical Analogy

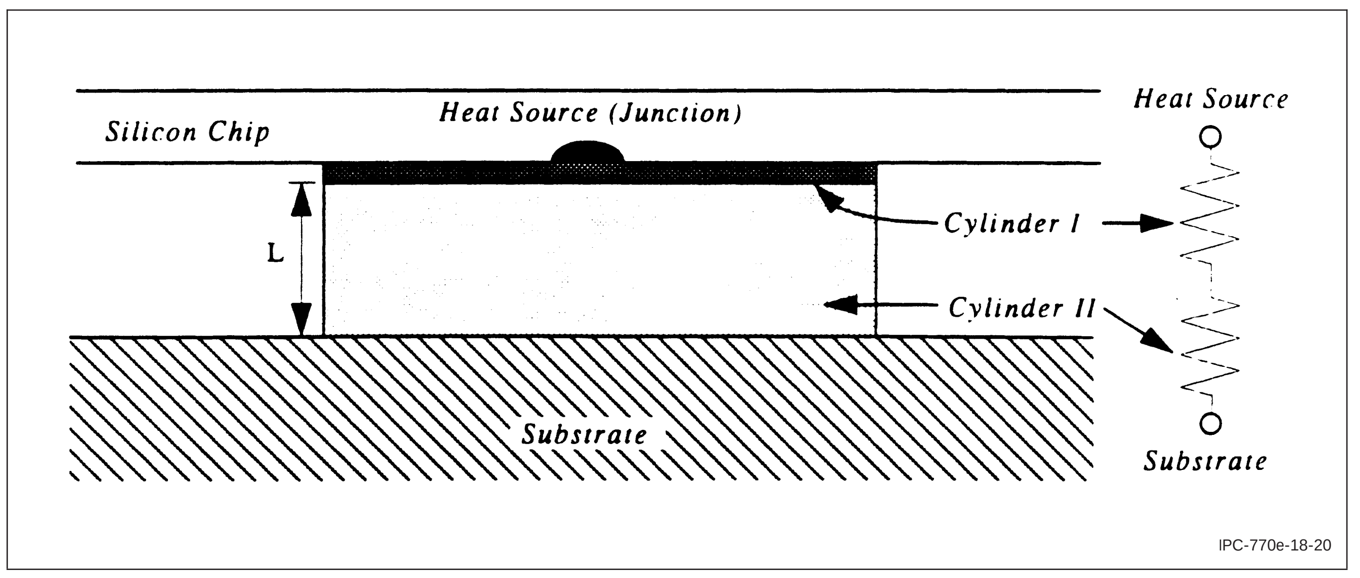


Figure 18-20 Bump Interconnect Equivalent Model

Table 18-3 Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip)

Interconnect Option	Diameter (m)	Cylinder I			Cylinder II			Total R (°C/W)
		L (m)	A (π^2) (nm^2)	R (°C/W)	L (µm)	A (π^2) (nm^2)	R (°C/W)	
Option A	150	10	18	550	75	18	116	666
Option B	125	10	13	762	63	13	135	897
Option C	100	10	8	1238	50	8	174	1412
Option D (DCA)	150	10	18	550	≥75	18	≥116	≥666

chip scale packaging for highly specialized thermal conduction packages. Supplemental features like thermal paste can be added to enhance thermal performance. Other materials like chip underfill used to improve reliability also alter heat dissipation. All these components influence the junction to case thermal models.

18.3.16.2 Thermal Paste Model The thermal paste is applied to the chip backside to reduce the thermal resistance between the chip and package lid, as shown in Figure 18-21, or heat sink. The approximate thermal model is shown in Figure 18-22.

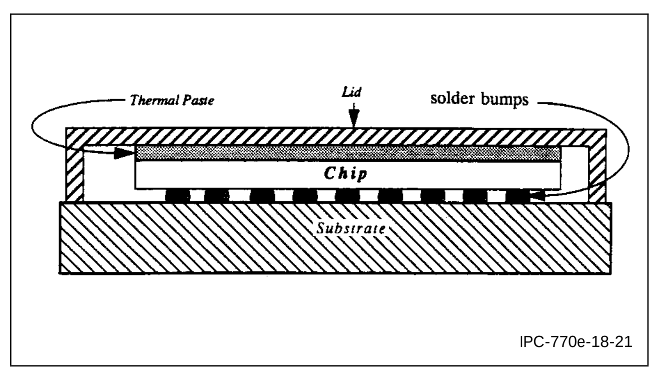


Figure 18-21 Thermal Paste Example

18.3.16.3 Chip Underfill Chip underfill is used to enhance reliability for flip chip and some grid array packages. It is dispensed between the chip and substrate surrounding the bumps as shown in Figure 18-23.

Because it completely fills the gap between the chip and substrate, it does change the thermal model. The approximate model is shown in Figure 18-24.

18.4 Handling, Shipping and Storage Bumped dice are shipped using tray, waffle packs, tape and reel, and wafer frames depending on flip-chip assembly method. A temperature-controlled dry air environment is necessary for proper storage and handling.

18.4.1 Handling Systems

18.4.1.1 Bare Die Manually handled with tweezers.

Caution: Without proper training, there can be tweezer damage to the die.

18.4.1.2 Reels In cans or sealed bags. Usually automatic pattern recognition handling equipment used for handling the die.

18.4.1.3 Waffle Packs Stacked until used. Low volume handling may be manual. High volume is automatic.

18.4.1.4 Frames Carrier racks. Usually automatic pattern recognition handling of die.

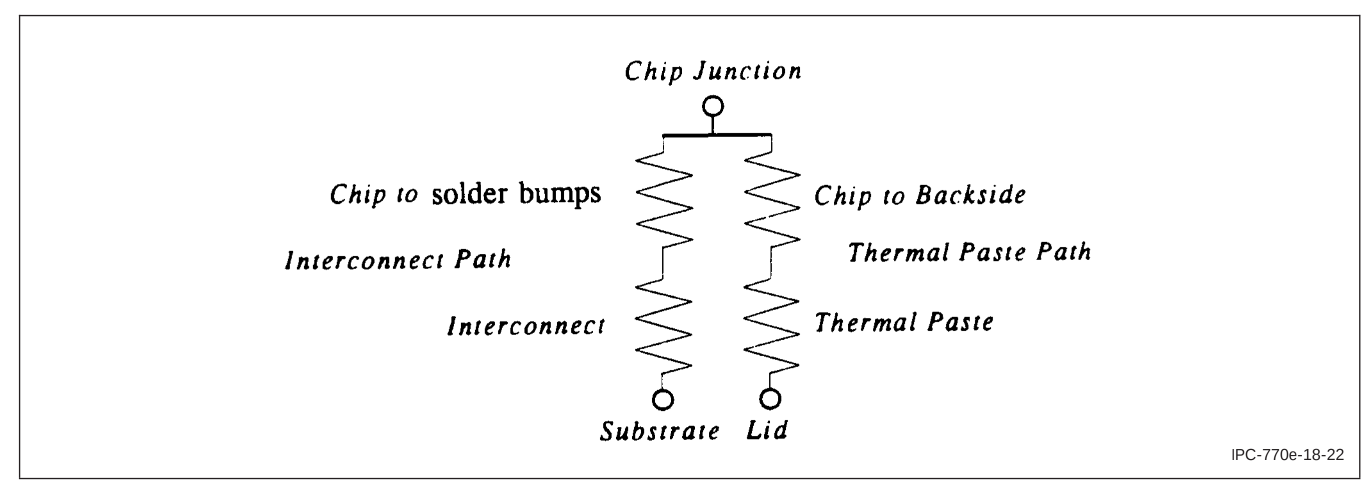


Figure 18-22 Appropriate Thermal Model for Thermal Paste

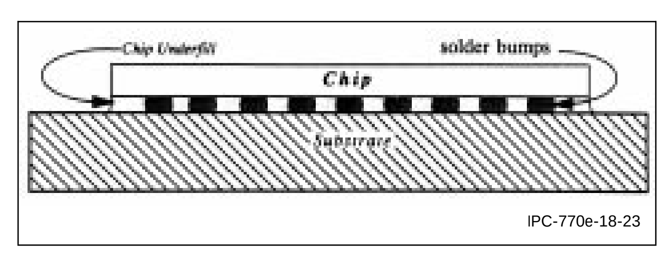


Figure 18-23 Chip Underfill Example

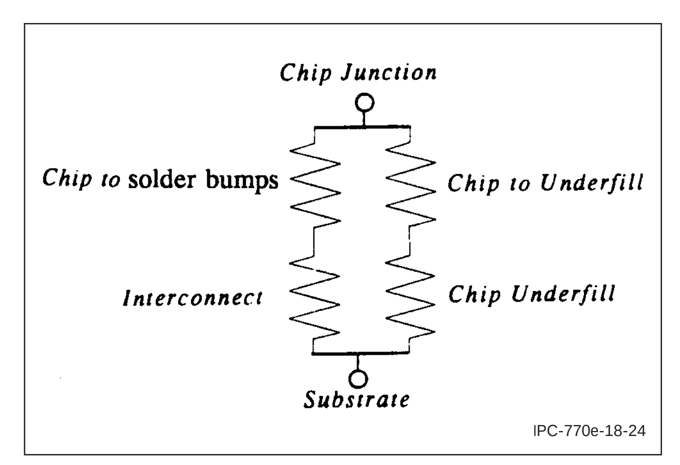


Figure 18-24 Approximate Thermal Model for Chip Underfill

18.4.2 Storage Atmosphere Nitrogen-purged atmosphere reduces assembly problems. Nitrogen atmosphere protects the bump from bump oxidation and bump corrosion. Oxidized solder bumps do not reflow properly at normal reflow temperatures. The dry nitrogen atmosphere also protects the bump from moisture and corrosion. The combination of chlorine contamination and moisture can cause corrosion on solder bumps. At elevated temperatures, the corrosion process is accelerated. For more information on storage and handling (see IPC/JEDEC J-STD-033).

18.4.3 ESD Protection ESD precautions must be taken during the handling of components, loading feeders, trays, etc.

18.4.4 Types of Carrier Packaging for Shipping

18.4.4.1 Bare Die Die that is usually manually handled with a vacuum pickup tool and placed on a manual die bond system for bonding to the Circuit Board. Usually done for first silicon engineering evaluations.

18.4.4.2 Waffle Packs The die can be manually or automatically placed in plastic square carriers with pockets for shipping to the customer.

18.4.4.3 Tape and Reel Die is automatically placed on a reel of tape with pockets to hold the die. The reel is then placed in a purged nitrogen bag for shipping.

18.4.4.4 Bare Die on Wafer Tape Frames The die is placed on a stretched frame of tape. The frames are placed in carriers for shipping to the customer.

18.4.5 Storage System and Length of Storage

18.4.5.1 Short Term, No Nitrogen Bare die/wafer carriers stored in cabinets with no nitrogen purging. Maximum storage time - 24 hrs. (This type of storage not recommended.)

18.4.5.2 Short Term with Nitrogen Bare die/wafer carriers stored in cabinets with nitrogen purging. Maximum storage time - two weeks.

18.4.5.3 Long Term Bare die/waffle packs, wafer carriers in sealed bags or sealed packages that have a nitrogen-purged seal. Maximum storage time - one year. Check package labels for max time.

18.5 Mechanical Properties The solder bump forms the electrical and mechanical bridge between the chip and next level assembly. It absorbs the stress between the chip and next level of assembly caused by variations in their relative thermal expansion rates.

18.5.1 Interconnect Joint Dimensions Common bump diameters and minimum pitches are shown in Table 18-5. Minimum pitch guidelines are based on radial distances (center to center) between bumps. Bump diameters are measured at the widest point of the ball. It should be noted that 250 µm pitch is the most commonly used for the evaporative and electrodeposited bump process, due to its ease of manufacture and smaller pitch capability; 225 µm pitch is used for very high interconnect density applications. Generally the larger bumps provide improved reliability.

Table 18-5 C4 Bump Diameter and Minimum Pitch Options

Deposition Types	Diameter (µm)	Minimum Pitch (µm)
(A) Evaporation or Electrodeposition	150 µ 125 100	300/350 250 225
(B) Screen Printing	200 150 125	375 250* 200*

*peripheral only

Today, for flip chip applications, minimum pitch requirements are larger to account for printed board wiring capabilities. An example of typical DCA bump design is shown in Figure 18-25.

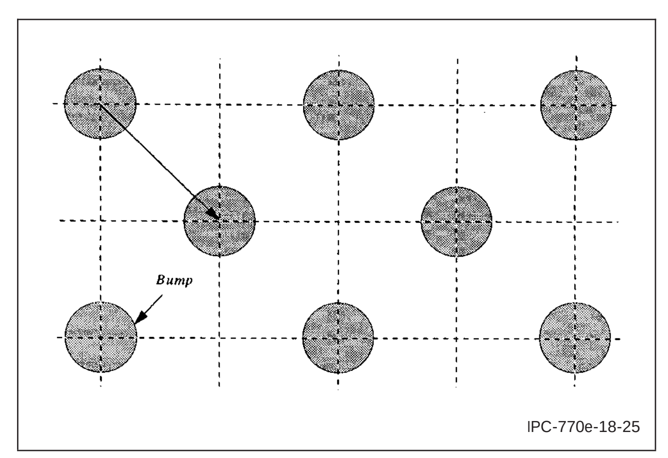


Figure 18-25 Recommended DCA Grid Pitch (250 µm Grid, 150 µm Bumps)

18.5.1.1 Volume of Solder Affects Solderability and Reliability Generally the larger bumps provide improved reliability.

18.5.1.2 Solder Coplanarity Affects Assembly Yields Coplanarity is a critical parameter in achieving sound solder joints. The maximum variation in coplanarity throughout a component's lead configuration is generally accepted to be 0.1 mm. A solder paste height for fine pitch components is usually about 0.15 mm. This provides very little margin of error for lead coplanarity with an average penetration of the lead into the solder paste of 65%. When leads are out of plane, unsoldered joints result because the solder paste cannot contact the high leads, or weakened joints may result from low solder joint cross-sectional area.

Coplanarity must be an acceptance criterion for component procurement. Incoming inspection of components may include AQL inspection for coplanarity characteristics or the supplier may be certified. Capability of placement machines to inspect for planarity is a highly desirable feature to accept or reject components on an individual part level.

A contributing factor to part coplanarity is the planarity of the circuit board pads. The finish on the circuit board is a key factor in achieving a flat mounting pad. Hot Air Solder Level (HASL) surface has excellent solderability but the planarity of the pads varies with the thickness of the HASL coating. This variation may be as much as 0.075 mm, depending on board layout, pad design and HASL process characteristics.

Solder or tin plated surfaces have planarity equivalent to the underlying copper surface, but plated solder is porous and tin coatings become difficult to solder with age. Copper anti-tarnish surfaces are now becoming available. This finish retains the planarity of the copper surface with good shelf life but may require some adjustment of the flux or solder paste to ensure solderability.

Other options for flat surface finishes are immersion gold, electroless Ni, immersion silver, or immersion tin.

18.5.2 Solderability of Bumps Not Wetting or Partial Wetting to Substrate is a Reliability Concern Solderability of components must be maintained by avoiding storage in corrosive atmospheres or excessive heat. Severe oxidation of the lead finish or formation of excessive intermetallics results in weak or incomplete solder joints. Humidity, in addition to causing plastic component body cracking, accelerates the degradation of the lead solderability. In the case of leads with a solder finish over copper, exposure to temperatures of 125°C adds approximately 0.5 µm copper-tin intermetallic per day. When the intermetallic thickness approaches the solder thickness, solderability is degraded. The high tin content on component leads being supplied by many manufacturers is more susceptible to this problem and often requires aggressive flux to achieve acceptable solder joints.

18.6 Electrical Issues In the case of ICs, many characteristics of quality such as high speed performance and long term reliability are difficult to ascertain prior to packaging the component. IC manufacturers traditionally check the devices on a wafer for functionality, package the functional devices in single chip packages and address performance and reliability issues at package level testing.

By eliminating the first level of packaging, the chip manufacturer must address the issues of IC performance and

reliability at the bare die level. Addressing these issues at the level of a MCM results in a yield reduction. Therefore, more stringent component-level test strategies coupled with cost effective rework processes is required for successful known good die manufacture.

Several techniques are available for contacting the die while performing full at-speed functional test and burn-in stress. These include both soft connection (metallurgical) and mechanical connection of the flip chip bumps, metallized bond pads and posts to a Known Good Die (KGD) carrier.

18.6.1 Wafer Test/Sorting Inked Die The most common process is to test the wafer, ink the die and visually take out the inked die. However visual sorting of the die is subject to error and bad die are sent on. Die can be sorted from expanded wafer frame or none expanded.

18.6.1.1 Wafer Ink Dotting vs. Wafer Mapping The newer preferred method is to test the die with computer wafer mapping. The computer wafer map is then used to take out the inked die.

18.6.2 Room Temperature Testing of Wafer vs. Testing Wafers over Temperature and Costs Testing wafers over temperature is more costly than testing packages over temperature. A good design with known temperature compensations can avoid testing over temperature. However, some IC processes defects cannot be tested out at room temperature. The IC process defect level should be known and the process monitored.

18.6.2.1 Known Good Die (KGD) Issues - Guarantee of Good Electrical Die to Assembler (Acceptable PPM Defect Levels) Known Good Die can help to eliminate the need for rework due to die reliability.

Cost modeling can be performed to determine whether an advantage exists for using KGD in a given application. The models account for such factors as number of die in the board, rework costs, and bare die test and burn-in yields. Factors must be considered such as the complexity of the die in the board and whether it is possible to test and burn-in at the board level. Additional applications for KGD exist such as use in Direct Chip Attach (DCA) applications where chip rework may be unavailable. Single-chip module use of KGD may be effective early in the life of a program when die yields are low and the die is placed in an expensive package.

The dramatic increase in available computer power has enabled application of a variety of yield improvement techniques that were previously too data intensive to be cost effective. Extensive use of Statistical Process Control (SPC), Automatic Test Generation (ATG), and fault simulation is now practical. These and other tools can resolve many of the manufacturing problems associated with flip-chip production.

The three prime concerns of all manufacturing disciplines are component quality, process control and finished product verification. Each presents unique challenges to the successful production of flip-chip technology. These challenges are inherent consequences of the flip chip advantages of high density and elimination of the first level of Integrated Circuit (IC) packaging.

The quality of the components and materials of which it is made limits the quality of any manufactured product. The upper limit for the yield of any collection of components is the product of the individual component yields.

18.6.2.2 Testing Individual Die After Die Sort - Additional Cost of Testing vs. Yield Improvement to Customer. (PPM Defect Levels) This is a very costly process but guarantees very low PPM defects to the customer.

18.7 Marking The die themselves cannot be marked with organic inks. Marking inks can contaminate the interconnect joints and cause solderability/reliability problems.

18.8 Physical Conditions

18.8.1 Workmanship Refer to IPC-HDBK-001 ‘‘Soldering Handbook,’’ IPC-HDBK-610 ‘‘Handbook and Guide to IPC-A-610,’’ and IPC-A-610 ‘‘Acceptability of Electronic Assemblies.’’

19 MOUNTING STRUCTURE GUIDELINES FLIP CHIP DIRECT CHIP ATTACH (Refer to General Guidelines Section)

20 ASSEMBLY HIERARCHY FLIP CHIP DIRECT CHIP ATTACH

20.1 Process Steps Flip chip assembly mount sequence of events is as follows:

- Clean substrate pattern
- Preheat
- Flux - print flux on substrate or dip flip chip in flux
- Placement and attach
- Reflow
- Cool down
- Clean chip/substrate (optional)
- Underfill process
- Chip coating

20.2 Manual Techniques for Semiautomated Pick and Place Manual Placement of Flip Chips is a low volume assembly process. This is most commonly done with Flip Chips in waffle packs or bare die wafer frames. This is

done on a manual pick and place bonder with an operator. Each die is manually aligned, with mirrored optics, to the substrate finger pattern. It is then placed on the board/substrate. This is usually done for engineering first silicon evaluations with no production intent.

20.2.1 Dexterity The set up time is much shorter than for the automatic systems and allows for more flexibility of different die and substrates.

20.3 Automated Techniques Automatic placement of flip chips is for high volume, fast attachment assembly process. High volume flip-chip carriers are precision waffle packs, die on reels, or bare die on expanded wafer tape frames.

20.3.1 Types of Equipment The equipment is usually an automatic die transfer with pattern recognition for placement of the die on the substrate finger pattern.

20.3.2 Precision The high volume equipment has more precision alignment because of the pattern recognition system.

20.4 Single Point Attachment Not applicable to this process.

20.5 Mass Attachment Properties Some common methods used are provided below.

20.5.1 Convection Oven Solder Reflow The part goes through a belt furnace with heating zones and forced gas flow for even oven temperature.

20.5.2 Vapor Phase Solder Reflow The substrates go through a vapor solution that is at the reflow temperature. This process is being phased out for environmental reasons.

20.5.3 Infrared Solder Reflow The parts may be on a walker or belt where infrared light heats the part. Since infrared lights are at a much higher temperature than the solder reflow, the parts must be monitored for proper reflow temperature profile. Variables are distance of part from lights, belt speed, and reflectivity changes of parts and condition of oven lights.

20.5.4 Profile Analysis There are four temperature zones:

- Preheat
- Soak/Flux Activation
- Reflow
- Cool down

20.5.4.1 Oven Solder Reflow The preheat up should be a slow ramp up to reflow temperature. This rise should be less than 2.5°C/sec. The soak zone is a flat temperature zone 60-120 sec before the reflow zone temperature. This zone is where the flux activates. The flux reduces the oxide on the solder balls and causes the solder mixture to bond at reflow temperatures. At the reflow temperature zone, the solder is heated above liquidus temperature. This is a quick spike temperature zone. An optimum time should be 30-60 seconds above the Liquidus temperature, and the peak temperature should not exceed 35°C above liquidus. These temperature/time combinations keeping solder intermetallics to a minimum. Cooling too fast induces excess thermal stress due to board warpage. The solder structure looks rougher than normal with uneven cooling. An optimum reflow has smooth solder bumps.

20.5.4.2 Vapor Phase Reflow Profiling is typically not necessary but monitoring of the sump temperature is recommended. In modern systems, using a nonsaturation technology vapor phase reflow can slow down reheat. Older vapor phase systems typically have steep ramp-up temperatures because of inadequate preheat capability. This may be detrimental to some products. This process is being phased out for environmental reasons.

20.5.5 Nitrogen Reflow Atmosphere The nitrogen atmosphere should have a minimum of contaminants. Oxygen is the biggest contaminant to reduce fluxing action. There should be less than 200-PPM O2 contaminants in the reflow atmosphere. Maximum fluxing and proper cool down allows for round solder balls. This also keeps solder bump voids to a minimum.

21 CLEANING

In the case where printed board assemblies are to be conformally coated, the assembly should be free of flux residues and other contaminants prior to the application of conformal coating. The cleaning agent(s) used for the removal of grease, oil, wax, dirt, flux and other debris should be selected for its ability to remove flux residue, ionic, ionizable, nonpolar and particulate contaminates. The cleaning agent should not degrade the material and parts being cleaned (see IPC-CH-65, IPC-SC-60, IPC-SA-61 and IPC-AC-62).

21.1 General Considerations

21.1.1 Description of Process Cleaning involves the exposure of the soldered assembly to a liquid, or vapor/gas (or both) for a sufficient time and at a sufficient temperature to remove potentially harmful contaminants and with sufficient movement to extract unwanted particulate material. This may be followed, either by a sequence of secondary liquid immersions to remove the cleaning fluid and

contaminants before proceeding to the drying process that should remove all remaining liquid. Alternatively, drying may immediately follow removal from the cleaning liquid.

In some instances, gentle mechanical movement during cleaning may be augmented or replaced with ultrasonic agitation and/or pressurized jets of the cleaning liquid to assist flow through small orifices and in areas where small gaps exist. Pressurized air jets may be used to assist removal of liquids trapped beneath components.

21.1.2 Selection of Cleaning Materials No assumptions should be made concerning the compatibility of different cleaning materials as some combinations can have serious consequences.

Manufacturers and users should agree to standardize on known compatible materials within families of flux chemistries for both soldering and rework.

21.1.3 Frequency of Cleaning Cleaning should be undertaken after every independent soldering operation to ensure that any subsequent heating does not make assemblies harder to clean. Mechanized in-line processing equipment may not require this. Cleaning should be carried out as soon as is practicable after any soldering operation, e.g., within 15 minutes.

21.1.4 Ultrasonic Agitation Component specifications and assembly strength should be checked before applying ultrasonic agitation.

Cleaning systems applying ultrasonic agitation should not be used for Level C products containing cavity semiconductor packages or for any assembly having unsupported wire bonds to naked die unless specifically qualified and authorized by the user.

Large printed boards carrying many components and which may require several rework cycles should not be ultrasonically cleaned after each cycle. Local brush cleaning should be used for all except the final cleaning operation and, preferably, a ‘‘no-clean’’ or very low activity flux should be used at all times.

21.2 Cleanliness Assessment Wherever possible, testing a contaminant for functional effects should be performed under conditions similar to those of the expected working environment. The conditions represented in this clause and any related surface area calculations apply to both sides of the assembly.

Production facilities should have a standard based on how much of each type of contaminant can be tolerated. Testing with ionic extract equipment and insulation resistance testing under specified environmental conditions can provide a base for setting a facility standard. When others appear, or when there is a major change in levels, all abnormal conditions should be evaluated.

21.2.1 Flux Residues The following provides an approximate analogy between L, M and H type fluxes and the traditional classes of rosin-based fluxes and others such as water-soluble or synthetic activated fluxes:

- L0 type fluxes: all R, some RMA, some low solids (‘‘no clean’’)
- L1 type fluxes: most RMA, some RA
- M0 type fluxes: most RA, some low solids (‘‘no clean’’)
- M1 type fluxes: most RA
- H0 type fluxes: some water-soluble
- H1 type fluxes: all RSA, most water-soluble and synthetic-activated

Residues arising from the above fluxes include particulate, residue and corrosion residue and should be removed from the assembly.

21.2.2 Visual Inspection Immediate post-cleaning visual inspection should be carried out without magnification. If problems are seen, closer inspection using appropriate magnification may be used.

Contamination should be judged not only on cosmetic or functional attributes, but also as a warning that something in the manufacturing system is not working properly.

21.2.3 Solvent Extract Conductivity Measurement Totally immersing the assembly and measuring the change in conductivity of the liquid used can monitor average levels of residual ionic contamination for completed assemblies. Nonionic contaminants are not measured. This method is suitable for regular checking of production samples and can generate feedback data for process control within less than one hour.

For components with small standoff clearances, true levels of contamination can only be ascertained if these components are first partially lifted away to allow access to any trapped material beneath them - a destructive action. The melting of solder during partial lifting should be done without using a flux, as this brings an unwanted increase in the contamination level.

Solvent extract conductivity measurement should not be applied for assessing contamination levels after assembly using ‘‘no-clean’’ and ‘‘never-clean’’ fluxes.

21.3 Post-Soldering Cleaning When required, flux residue should be removed as soon as possible, but not later than one hour after soldering by applying cleaning agents. Some fluxes may require more immediate action to facilitate adequate removal. Flux used in the process of soldering is divided into three basic types. The type characterization is related to factors based on the corrosive or

conductive properties of the flux or flux residue. Flux are specified according to one of the following three types of flux/flux residue activity per J-STD-004:

- L = Low (or none)
- M = Moderate
- H = High

Mechanical means such as agitation, spraying, brushing, etc., or vapor degreasing and other methods of application may be used in conjunction with the cleaning medium. Ultrasonic cleaning may damage certain parts. Therefore, tests should be conducted to determine the applicability of the process.

The post soldering cleaning procedure should be as defined in J-STD-001, depending upon end product requirements and fluxes used as follows:

1. A rough cleaning step for the removal of most flux residues (ionic and nonionic) or
2. Step 1 followed by a fine cleaning step for the removal of the remaining flux residues (ionic and nonionic) or
3. Steps 1 and 2 followed by a final cleaning step that includes a solvent or solution removal operation for the removal of final traces of contamination.

Because of generally smaller spacing between leads, smaller clearances between the substrate and the component body and large area beneath the devices, chip carriers present a more difficult cleaning situation than through-hole mounted devices. Clearance under the package should be adequate to facilitate effective cleaning operation (see IPC-SC-60 and IPC-AC-62).

22 ELECTRICAL TEST CONSIDERATIONS

22.1 Five Types of Testing The following list describes five basic types of tests that can be performed on SMT boards:

- Bare-board test, which checks the unpopulated board for shorts and opens.
- Manufacturing defect analysis, which checks the populated board for soldering shorts.
- In-circuit test operational verification of each individual component.
- Functional test operational verification of functional block of circuits.
- Combination test limited integration of in-circuit and functional tests.

The first test type is a bare-board test, which is performed by the board fabricator. The remaining four test types are loaded on assembled board tests that are performed after assembly. The bare-board test should be mandatory, while the loaded board may be tested using any combination of the four loaded board tests.

22.1.1 Bare-Board Test In testing printed boards using through-hole technology, the defect rate and the test methods chosen are the principle determiners of overall test cost. Real-estate considerations (specifically the percentage of nodes that are available for bed-of-nails probing) are not a concern, since the holes provide 100% nodal access. In testing surface mount boards, however, real-estate considerations (in addition to defect rates) have an impact on test costs, since nodal access determines which test methods are possible and effective.

22.1.2 Assembled Board Test This method of test must be determined prior to design layout. If the defect rate is relatively high, most boards require diagnosis, and the economics of automatic in-circuit test (ICT) demand that full nodal access be provided within the board layout. If the defect rate is low, ICT may be omitted and rely on a functional test. Extremely low defect levels would theoretically allow 0% nodal access (no bed-of-nails test at all), applying only a simple pass/no-pass test through the edge connector, and throw away failing assemblies rather than diagnose them.

The major considerations in determining nodal access are:

- Defect rate
- Diagnostic capability
- Real-estate impact
- Board area
- Layer count
- Cost impact

Determining the percentage of nodal access to design into a board layout requires trading off all the issues discussed previously: defect rate, test development cost, test operation costs including manual troubleshooting costs and impacts on real estate. Short of having no defects at all, full nodal access remains the most desirable option.

As with through-hole technology boards, once the board is designed (nodal access fixed) and its tests are designed (test methods fixed), the defect rate becomes the primary key to reducing test costs. Therefore, defect reporting, analysis, and correction/prevention are imperative. This may involve closer supplier relationships to reduce component and board level problems, and in-house action to reduce process-induced problems.

22.2 Nodal Access In the early stages of product development cycles, test philosophies and strategies are often undefined. This is especially true when a company is moving from one level of packaging technology to a higher level of packaging technology. For example, if a company moves from through-hole technology to surface mount technology. During these transition periods, the concurrent engineering approach is essential for designing nodal access for testability into the product. Concurrent engineering is the principle vehicle by which test priorities can and

should be moved up to the beginning of the design cycle and addressed with a higher priority. In the early stages of a design, a test philosophy should be clearly defined, then a strategy for executing the tests can be implemented. An ideal philosophy to adopt is one that identifies all of the different test types and the level of test that each type requires.

22.2.1 Test Philosophy Should be written to encompass whatever combination of tests are necessary for the product. Then a simple strategy for implementing the required tests can be defined prior to beginning the design process. Planning testability at the beginning of a product development cycle instead of the end can result in significantly lower test costs per node and provide higher nodal accessibility throughout the entire process from initial design to final test.

The best test philosophy to adopt is one that makes provision for executing every test method available. Even if the product testing procedure is well defined at the beginning of the development cycle, it may change after the design is complete. Considerations should include:

- Strategic placement of all component vias.
- Provide access to every node of every net.
- Access every node from both sides of the board.
- Correct test pad geometry and clearances.
- Do not probe directly to SMT component lands.

Even in the densest designs, the philosophy of providing 100% access to every node of every net from either side of the board can be accomplished. However, this decision must be made at the beginning of a design.

22.2.2 Test Strategy for Bare Boards After the product test philosophy has been established, a test strategy or procedure can be defined. For an overview of several elements of a procedure, consider the following:

- Vision inspection of inner layers using AOI.
- Vision inspection of O/L land/via connections.
- Probe only vias on either side for bare board test.
- Damage to SMT lands with probe tips.
- Probe secondary side vias for loaded test board.
- Screen paste on vias for airtight board.

The actual product test strategy must be organized by all of the concurrent engineering team members who are involved in the testing process. This ensures that the integration of the various test types and procedures do not have too much redundancy, or create gaps that may endanger test integrity.

22.3 Full Nodal Access for Assembled Board The number of test probes needed to test the board is equal to the total number of device nodes or common connection between devices. However, in the case of most dense surface mount designs, this often requires the use of a double-sided (or ‘‘clamshell’’) test fixture because all of the nodes are not accessible from one side of the board.

The ICT only needs to have access to one node per net. Every net has at least two nodes. Some nets have many nodes; for example, on memory boards one net may be connected to many nodes. In order to achieve full integrity at the ICT level, access to only one node of each net is all that is required. Therefore, the total number of test probes required to perform the ICT is significantly less than the number required for the bareboard test.

The use of design concepts with grid-based 100% nodal access from either side of the board may be the most economical approach from the total process perspective. If the grid-based test land concept is used, the test fixtures for bare and assembled board tests do not become obsolete through later board connectivity revisions if the test nodes are not moved. Also, if the printed board uses buried vias, the grid-based test land concept with 100% nodal access may provide access to buried nets from the ends of the nets, this is a benefit realized during the bare-board test.

For fine-pitch components, it is good design practice to distribute approximately half of the test vias to the inside of the land pattern and the other half to the outside of the land pattern as shown in Figure 22-1. This accomplishes two objectives:

- The maximum density of test points is not exceeded.
- Wider distribution of test points reduces the high-pressure point areas, which causes fixture bowing during vacuum or mechanical actuation.

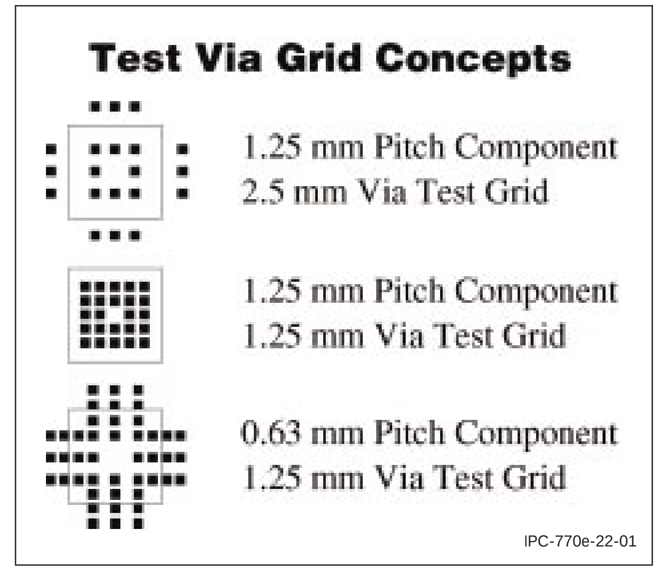


Figure 22-1 Test Via Grid Concepts

22.3.1 In-circuit Test Accommodation Specific via lands and holes can be accessed for automatic in-circuit test (ICT). The via land location for each common network

in a circuit is matched to a test probe contact in the test fixture. The test system can then drive each device on the assembly and quickly locate defective devices or identify assembly process problems.

To ensure precise alignment of the probe contact pins with the printed board, exact probe position and specific networks must be furnished to the fixture developer. Identifying the test locations as components in the CAD data base allows for easy transfer of fixture drilling data. This data reduces fixture development time and eliminates the drilling of excessive, nonfunctional holes in the fixture base.

22.4 Limited Nodal Access Limited nodal access (less than 100%) still allows the use of ATE spring probe (bed-of-nails) testing, but not as effectively as full nodal access does. As soon as nodal access goes below 100%, shorts, defects and in-circuit testing cannot be performed completely, and so some of these faults survive to complicate later testing. At bed-of-nails functional test, there is increased manual probing, because (1) not all shorts, manufacturing defects, and I/C failures were detected earlier, and (2) fewer internal nodes are ‘‘visible’’ through the fixture.

A greater burden is therefore placed on functional or system test to detect and diagnose shorts, defects, and bad devices. This burden varies inversely with the nodal access percentage. The extra effort at functional test may consist of additional recurring manpower cost to diagnose failing boards, or it may mean developing a more detailed functional test (nonrecurring cost) than would have been planned otherwise.

22.5 No Nodal Access No nodal access (0%) prohibits bed-of-nails testing and defers all assembly defects and component testing until the functional or system test bed. This can only be cost-justified if the much higher cost-per-defect repair is performed so infrequently that the total cost is less than the cost of developing and operating an ATE bed-of-nails test. In other words, the first pass yields must be extremely high to justify this approach.

22.6 Clam-Shell Fixtures Impact Probing the printed board from both sides requires a ‘‘clam-shell’’ type of fixture. These fixtures are expensive, take more time to fabricate, require larger test lands on the primary side to protect against registration problems due to tolerance stack-ups, and are more difficult to maintain.

22.7 Printed Board Test Characteristics

22.7.1 Test Land Pattern Spacing Design for testability is as much a part of the schematic design process as it is a part of the board layout process. Ideally, the printed board would have 100% of the nodes accounted for on the secondary side. In-circuit testers must have access to at least one node per net. Probe spacing is optional; however, standard probe spacing is typically 2.0 mm to 2.5 mm while middle probes can be spaced as close as 1.0 mm to 1.25 mm.

The drawbacks to the 1.0 mm to 1.25 mm grid-based test lands are the following. Spring probes are more expensive. They do not hold up as well in high-volume production. Also, any vias used as test points should be solder filled for better contact and increased probe life.

22.7.2 Test Land Size and Shape Lands or vias should be 0.9 mm to 1.0 mm for probing. As land sizes decrease, misses increase dramatically as shown in Figure 22-2. The use of square via lands may provide a larger target zone for the test probe to contact.

22.7.3 Design for Test Parameters The following considerations are also important to the general land pattern design and should be incorporated into the printed board:

- Two unplated tooling holes should be available on diagonal corners of the printed board.
- Test lands should be 2.5 mm minimum from the edge of the printed board to facilitate gasketing on vacuum fixtures.
- When using vias for test points, caution should be taken to insure that signal quality is not degraded at the expense of testing capability.
- Test lands should be 0.63 mm minimum from mounting land areas.
- It is useful to mark the test vias and lands on an assembly drawing in event of the need to modify the circuit topology. Changes made without moving test lands avoid fixture modification, saving cost and time.
- Where possible, provide numerous test lands for power and ground.
- Where possible, provide test lands for all unused gates. Free running gates sometimes cause instability during in-circuit testing. This provides a means of grounding these spurious signals.
- It is sometimes desirable to provide drive and sense nodes test lands to perform six-wire bridge measurements during in-circuit test. Directions for this should come from test engineering.
- Care should be taken when mounting components on the secondary side to avoid covering a via that is a designated test land. Also, if a via is too close to any component, damage may result to the component or fixture during probing (see Figure 22-3).
- To minimize rework and hence maintain high reliability, the electrical test program should include both ‘‘in circuit’’ and full functional testing, or equivalent Boundary Scan and other tests.

Probability of at Least One Miss
100%
80%
60%
40%
20%
0%
0.25 mm 0.35 mm 0.5 mm 0.6 mm 0.75 mm 0.9 mm 1.0 mm
Diameter
Test/Via Probe Contact Size
1.0 mm Dia [0.04"]
0.9 mm Square [.036"]
IPC-770e-22-02

Figure 22-2 General Relationship Between Test Contact Size and Test Probe Misses

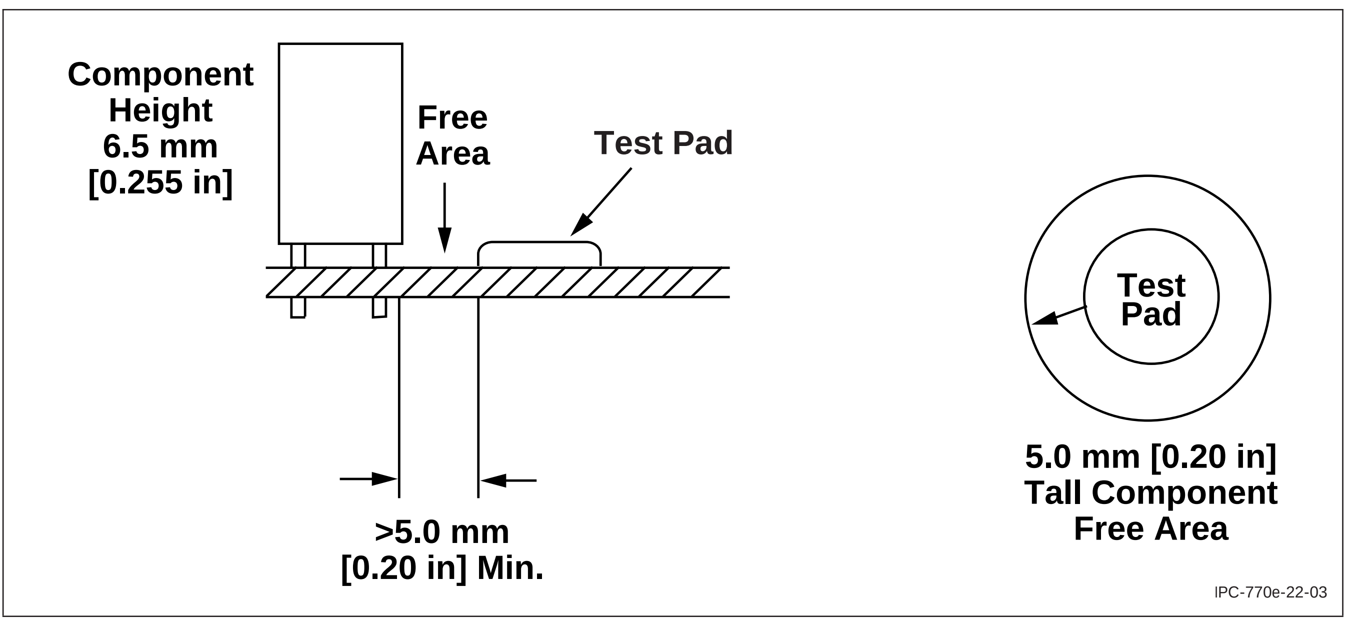


Figure 22-3 Test Probe Feature Distance from Component

22.7.4 In-Circuit Test Whenever practicable, to minimize probe length the board design should enable this test to be carried out entirely on the ‘‘low profile’’ side of the board. By avoiding the need for a clamshell fixture and the use of delicate long-throw probes, test result reliability is improved and probe life is extended.

For mixed technology with single pass soldered assemblies and for double-sided assemblies receiving more than one solder pass, it is good practice to perform an initial in-circuit test on all those components soldered during the first pass. If the board layout does not permit a single test on the low profile side after the second soldering pass, a

further probe test would be carried out. This approach may require extra jigging, but it can improve product reliability by making rework easier.

Where the quantity of through-hole components on a mixed technology board is small, manual probing is appropriate.

Depending on the user specification, for level C products containing more than 50 surface mounted components, the use of ''in circuit'' or equivalent Boundary Scan testing may be required.

22.7.5 Functional Test Normally functional testing is carried out via outgoing connections on the assembled board and no special mechanical precautions are needed.

22.7.6 Test Probes and Probe Lands The board layout should include probe test lands enabling surface mounted components to be tested after part or full assembly and without contact with their bodies or leads. Whenever practicable, test software should be designed so that components can be checked for parametric value and function. When this is not practicable, ''in circuit'' testing for connectivity and orientation is the minimum requirement.

The minimum distance between any two probes on a probe matrix board should be sufficient to enable the use of robust and reliable probe systems, particularly for volume production. To achieve this, the minimum spacing between probe centerlines, and hence maximum probe diameter, depend on the required protrusion length from the matrix board.

For example, the minimum probe centerline spacing should be 2.5 mm and the probe protrusion is 10 mm when the maximum height of components is 6 mm. That allows for clearance and board bow and twist. This does not necessarily imply the use of a 2.5 mm grid.

23 QUALITY ASSURANCE

The goal of quality assurance is to prevent nonconformance. A high amount of nonconformance means low yields, wasted materials, labor, and capacity, high probability of shipping nonconforming products (i.e., greater opportunity for defect screening efforts to fail), high inspection cost, high rework cost and higher than necessary cost over the long run. A quality assurance strategy consists of the following elements:

23.1 Relationship to Test/Inspection

23.1.1 Visual Inspection Prior to soldering, unsoldered assemblies should be examined to ascertain that no damage has occurred during transit or handling, and that component mounting is in accordance with the appropriate requirements.

When, for any reason, a component lead is terminated so that the lead is allowed to stress the soldered joint, the working of the joint has been observed to result in the generation of cracks that tend to relieve the stresses. In its ultimate condition such a connection, with extended cracks and discontinuities, might result in a fractured joint.

These connections are called ''disturbed joints.'' In the past they were called ''cold solder joints.'' The consensus is that cracking is usually caused by mechanical stress on the joint, which may be induced either mechanically or thermally. Component mounting impacts such as design established mismatches or component lead forming can create mechanical or thermal conditions that cause cracking. Some examples are:

- A component (such as a power transistor or module) mounted flat on the surface of a board with nonplated holes. In this case, the differential in coefficient of expansion between the board material and the lead material acts directly on the solder joint.
- Unsupported holes much larger than the component leads cause the solder fillet to thin out on one side of the hole to 0.1 mm or less. This situation is particularly noticeable when clinched leads are used.
- The use of eyelets in interfacial holes causes a thermal coefficient mismatch between the board material and eyelet.
- Care should be taken in clinching leads to ensure that straightening does not reduce the stress-relief bends.

Parts that generate heat, if mounted directly on the board, can cause locally severe thermal coefficient mismatches and result in cracking. All finished assemblies should be examined. The solder joint should indicate evidence of wetting and adherence where the solder blends to the soldered surface, forming a small contact angle; this indicates the presence of a metallurgical bond and metallic continuity from solder to surface.

Smooth clean voids or unevenness on the surface of the solder fillet or coating are generally acceptable. A smooth transition from land to connection surface or component terminal should be evident. The solder fillet should appear to be concave. The solder joint connecting the component should be examined for evidence of the following characteristics:

- ***Bridging –*** Solder shorting, or the spanning by solder, of section(s) that should be open between two or more conductors and/or component terminals.
- ***Webbing –*** A continuous film or curtain of solder parallel, but not necessarily adhering, to a surface or between separate sections of circuitry, that should be free of solder.
- ***Ball –*** Small spheres of solder adhering to laminate, mask and/or conductor surfaces.

- ***Sticking –*** Tiny balls, flecks or specks of solder adhering to laminate or resist.
- ***Slivers –*** Portions of tin-lead (solder) plating overhang on conductor edges partially or completely detached.
- ***Whiskers –*** Slender acicular (needle-shaped) metallic growth between conductors and/or lands.

23.2 Standard Magnification Verification inspection should consist of the following:

- Surveillance of the operation to determine that practices, methods, procedures and a written inspection plan are being properly applied.
- Inspection to measure the quality of the product.

Deviations from the prescribed inspection procedures, or practices that might have an adverse effect on the quality of the product should be noted and corrective action taken, as appropriate.

23.2.1 Magnification Aids for Examining Printed Board Assemblies The tolerance for magnification aids is ± 15% of the selected magnification power. Magnification aids used for inspection need to be appropriate with the item being processed. Lighting needs to be adequate for the magnification aids used. The magnification used to inspect solder connections is based on the minimum width of the land used for the device being inspected. When magnification is required by contract, the magnifications in Table 23-1 apply.

Table 23-1 Inspection Magnification

Land Widths or Land Diameters	Inspection Magnification Power	Referee Magnification Power
>1.0 mm [>0.039 in]	1.75X	4X
>0.5 to 1.0 mm [>0.020 to 0.039 in]	4X	10X
0.25 to 0.5 mm [0.00984 to 0.020 in]	10X	20X
<0.25 mm [<0.00984 in]	20X	40X

Referee conditions are used to verify product rejected at the inspection magnification power. For assemblies with mixed land widths, the greater magnification may be used for the entire assembly.

23.3 Process Control Used to continually identify variation of the end product through control and reduction of variation upstream in the process. It is a legitimate method to be used by management throughout the company to achieve quality improvement, reduction in costs, and increased customer satisfaction. Experience has shown the implementation planned, directed, and applied in a methodical way on a project-by-project basis has a higher probability of success. Elements of a process control system should address such areas as methods to demonstrate process capability, inspection and verification strategies, corrective action, and training and audit guidelines.

Statistical Process Control consists of statistical methods and procedures used to document and assure compliance with requirements.

23.3.1 Corrective Action Limits Should be established when implementing a process control system for product acceptance. The action limit is the threshold whereupon corrective action is initiated. When a process control plan is not used, the corrective action limit (threshold) is the point where the quantity of defects exceeds 0.3% of the opportunities for their occurrence.

Quality assurance is an ongoing procedure that should begin as materials and components are accepted on delivery. Consequently, certain quality assurance tests and inspections relating to assembly processes should be completed before any components are placed or soldered. These include solderability, surface cleanliness and coating quality.

Following assembly, the product should be inspected for defects and other workmanship features and then verified against the standard agreed upon between customer and vendor. Functional and quality tests, both mechanical and electrical, should be a part of this process. The ‘‘as produced’’ quality of a product is not maintained unless adequate handling procedures are operative. Care should be taken to ensure that tests and testing reflect the desired end product quality and that subsequent to acceptance nothing is done to degrade this quality.

23.3.2 Process Control Details Process control should be a documented system, available for a review that meets the intent of IPC-9191 or other user-approved system. The primary goal of process control is to continually reduce variation in the processes, products, or services to provide product or processes meeting or exceeding customer requirements. The process control system should include the following elements as a minimum:

- Training should be provided to personnel with assigned responsibilities in the development, implementation, and utilization of process control and statistical methods that are commensurate with their responsibilities.
- Quantitative methodologies and evidence should be maintained to demonstrate that the process is capable and in control.
- Improvement strategies to define initial process control limits and methodologies leading to a reduction in the occurrence of process indicators in order to achieve continuous process improvement.
- Criteria for switching to sample-based inspection should be defined. When processes exceed control limits, or

demonstrate an adverse trend or run, the criteria for reversion to higher levels of inspection (up to 100%) should also be defined.

- When defect(s) are identified in the lot sample, the entire lot should be 100% inspected for the occurrence(s) of the defect(s) observed.
- A system is in place to initiate corrective action for the occurrence of process indicators, out-of-control process(es), and/or discrepant assemblies.
- A documented audit plan is defined to monitor process characteristics and/or output at a prescribed frequency.

Objective evidence of process control may be in the form of control charts or other tools and techniques of statistical process control derived from application of process parameter and/or product parameter data. This data can be acquired from sources such as inspection, nondestructive evaluation, machine operation data, or periodic testing of production samples. For attribute data, the key is understanding and controlling parameters in the process that influence the response in question and establishing controls at that point. Attribute data, measured in PPM nonconforming product, can generally be correlated to a process capability index (Cpk) generated using variable data.

23.3.3 Defect Reduction Continuous process improvement techniques should be implemented to reduce the occurrence of defects and process indicators. When processes vary beyond established process control limits, corrective action should be taken to prevent recurrence. When corrective action is ineffective within 30 days of implementation, the problem should be referred to plant management for resolution.

23.3.4 Variance Reduction All variances from the guidelines of this specification should be minimized with the goal of elimination (where economically practical) through process corrective action. Failure to implement process corrective action and/or the use of continually ineffective corrective action should be grounds for disapproval of the process and associated documentation.

23.4 Process Verification Inspection Where required, verification inspection should consist of the following:

- Determination that the manufacturer has an acceptable documented quality control system.
- Surveillance of the operations to determine that practices, methods, procedures and inspection plans are being properly applied.
- Deviations from the prescribed procedures, or instances of poor practice, which might affect the product quality, should be noted and failure to promptly correct the deficiencies may be cause for suspension of acceptance until correction has been made or until conformance of the product to prescribed criteria has been demonstrated.

23.4.1 Workmanship The inspection criteria for workmanship should be fully established and agreed to, both interdepartmentally and between customer and vendor. Photographic or sketch arbiter examples are almost essential (see J-STD-001 for the complete and current requirements).

23.4.2 General Modification/Repair The following general modification and repair procedures focus on the preparation of printed board and printed board assembly surfaces for printed board substrate of conductive pattern modifications and repairs.

The following general modification and repair procedures focus on the preparation of printed board and printed board assembly surfaces for printed board substrate of conductive pattern modifications and repairs.

23.4.3 Destructive Testing Coupons are usually used for destructive testing. They are incorporated into the assembly panel and populated at the same time that the assembly is manufactured. Figure 23-1 shows an example of several coupons that can be used to evaluate component placement as well as cleanliness testing.

Destructive testing includes thermal and mechanical cycling as well as exposure to highly accelerated stress testing (HAST) environments.

23.4.4 Mild Burn-In (24 hr per assembly) Inspection levels are instituted to ensure those quality assurance aspects of electronic assemblies are inspected for conformance to IPC-A-610.

24 PERFORMANCE/RELIABILITY EVALUATIONS

There are several standards and guidelines that can assist in the development of electronic assemblies and their reliability for intended use. The IPC-D-279 deals with the design issues that address reliability expectations. In addition, reliability testing requirements for solder joint attachment can be found in IPC-SM-785. That standard identifies nine end-use environments and the expected probability of solder-joint failure over three separate time periods: one year, three years and five years.

24.1 Relationships to Test and Quality Assurance For component mounting, the major concern is one of accurate placement and assuring that the land pattern can accommodate the component footprint. There are many reliability tests that help evaluate the final assembly in order to insure that it meets the customer expectations. However, these tests are performed after attachment and cleaning processes.

Sometimes the failures that occur during these tests can be correlated back to the component mounting process. These characterizations normally relate to the deposition of solder

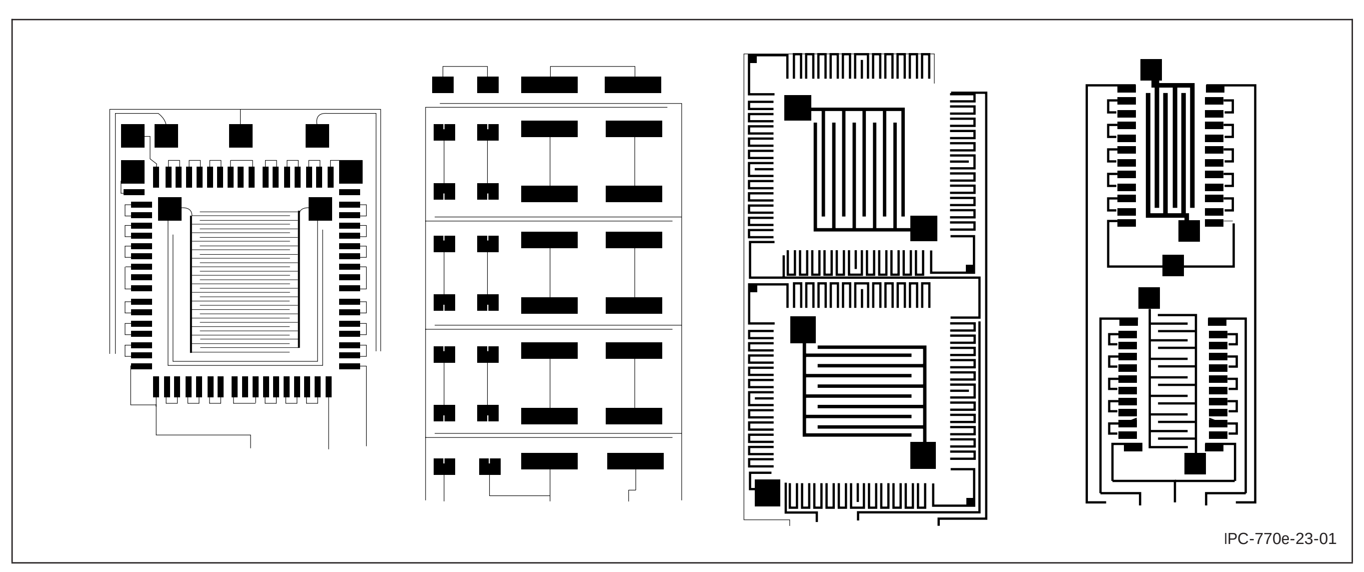


Figure 23-1 Destructive Testing Coupons

paste, flux used in the process or the component placement accuracy. When these nonconforming situations occur corrective action should take place. Some of the tests are:

- Highly Accelerated Stress Testing (HAST)
- Moisture
- Temperature Cycling
- Accelerated Burn-In
- Powered on Full Electrical
- Shock and Vibration
- EMI Protection

25 REPAIR/REWORK

The repair/rework of surface mount assemblies requires special care in design and practice. Because of the small land geometries, heat applied to the board should be minimized. There are various tools available for removing components. Resistance heating tweezers are also used for removing surface mounted components. Various types of hot air/gas and IR systems are also used for removing surface mounted components. One of the main issues when using hot air/gas devices is preventing damage to adjacent components. There are four basic guidelines for successful rework:

- Good printed board layout design.
- Selection of the correct rework equipment or tool.
- Sufficient manual skill.
- Adequate training.

The formation of intermetallic compounds during reflow means that touching up some joints may do more harm than good, particularly in the case of components with sensitive termination materials.

Due to these changes in microstructure, joint fatigue life-as measured by the number of temperature cycles endured before fracture occurs-can be significantly reduced.

A compromise must be sought between the conflicting requirements of minimizing board area and ease of assembly, electrical test and rework. If components are too close, adjacent or replacement components can easily be damaged during rework. Nearby solder may be reflowed a second time, leading to reduced mechanical attachment strength and the risk of cold solder joints. For those components that have been attached with adhesive and wave soldered, sufficient clearance should be allowed around the devices so that they can be twisted through at least 60 degrees in one direction to shear the adhesive while all the joints are molten.

25.1 Reuse of Components Components that are reused typically are not covered by the component manufacturer's warranty.

The following is a list of devices that can be particularly sensitive to removal and reuse procedures:

- Multilayer ceramic chip capacitors.
- LEDs.
- ASICs in PLCC or quadpack format.
- Wave soldered precision resistors.
- Large SOICs (>16 leads).
- Wave soldered quadpacks.
- Any component for which the data sheet proscribes reuse

Successful removal of large multilead integrated circuit packages involves the use of hot gas or heated electrode tools. Sufficient clearance around the package to permit the rework head to completely surround the device is essential.

25.2 Heat Sinking Effects Large ground planes and heat sinks conduct heat away from the component being reworked. Extra heat, perhaps for longer periods, is then required which can lead to damage to components or the

board. The fact that the solder joints may not reach reflow temperature is no guarantee that the component or the board has not been overheated.

This is a design problem that must be addressed at the printed board layout stage. Wherever possible any component termination that may need rework, including leaded through-hole types, should be thermally isolated from any ground plane or integral heat sink by a short length of copper conductor.

25.3 Dependence on Printed Board Material Type To ensure minimum damage to the printed board during rework, the base laminate should be a good quality resin and reinforcement type with a high copper peel strength.

Where high packing density is required, the use of inferior laminates can easily lead to problems with lands peeling away during rework. This may result either in the scrapping of complete assemblies or expensive repair of damaged copper areas.

For boards having high thermal mass such as metal-cored types or those with large area ground planes, to avoid employing a tool with a high heat input rate, the use of a hotplate to provide background heating is essential.

25.4 Dependence on Copper Land and Conductor Layout If space on a board is at a premium or signal conductors must be kept very short, designers often route a conductor between adjacent device lands spaced at the pitch of the component device being placed. In such cases, conductors should be covered with a solder resist to minimize the risk of lifting conductors during rework operations.

Routing conductors between lands at 1.0 mm pitch and below increases the risk of damage to the conductors during rework operations.

25.5 Selection of Suitable Rework Equipment Before layout starts, the designer should establish the rework tools that are available in production. No single equipment exists which is both cost-effective and can do rework on all components without prejudicing their reliability. Assemblers may wish to place more weight on some requirements than others, depending on the application of the product and the following salvage priorities e.g.:

- The main printed board assembly.
- The component for its high cost or nonavailability of a replacement.
- Both board and component for reuse or analysis.

As many as three or even five different tools may be needed, as well as a variety of different heads for each. Each type of component has one or more rework techniques best suited to its removal and then replacement. These may be different.

25.6 Dependence on Assembly Structure and Soldering Processes Where boards have surface mount components on both faces, control over the rework process must prevent damage to joints or loss of components from the reverse face directly opposite those being reflowed, as well as adjacent items. In some instances it may be advisable to design for the use of adhesive on one face even for reflowed assemblies.

No matter which method and tool is used, all the controlling variables must be addressed before design starts. These include:

- The extra time spent by solder above its melting point due to the rework and whether this exceeds the maximum time specified by the component manufacturer or the board supplier.
- The maximum time-temperature combinations that the component body materials can withstand. These include the original soldering process as well as any rework/repair.

26 COATING AND ENCAPSULATION

The detail guidelines for coating and encapsulation procedures are defined in the following paragraphs.

26.1 Conformal Coating The material specification and supplier's instructions, as applicable, should be followed. When curing conditions (temperature, time, IR intensity, etc.) vary from supplier recommended instructions, the alternate conditions should be documented and available for review. The material should be used within the time period specified (both shelf life and pot life) or used within the time period indicated by a documented system the manufacturer (assembler) has established to mark and control age-dated material.

26.1.1 Application A coating should be continuous in all areas designated for coverage on the assembly drawing. The coating fillets should be kept to a minimum. When used, masking materials should have no harmful or degrading effect on the printed boards and should be removable without leaving a contaminant residue. Dimensioning specified for masked areas should not be decreased in length, width, or diameter by more than 0.8 mm by application of conformal coating.

26.1.1.1 Adjustable Components The adjustable portion of adjustable components, as well as electrical and mechanical mating surfaces such as probe points, screw threads, bearing surfaces (e.g., card guides) should be left uncoated as specified on the assembly drawing.

26.1.1.2 Conformal Coating on Connectors Mating connector surfaces of printed wiring assemblies should not be conformal coated. The conformal coating specified on

the assembly drawing should, however, provide a seal around the perimeter of all connector/board interface areas. Press-fit pins and connectors installed after conformal coating is applied should be exempt from the seal requirement.

26.1.1.3 Conformal Coating on Brackets The mating (contact) surface of brackets or other mounting devices should not be coated with conformal coating unless specifically required by the assembly drawing. However, the perimeter of the junction between these devices and the board and all attaching hardware should be coated.

26.1.1.4 Conformal Coating on Flexible Leads Components which are electrically connected to the assembly by flexible leads (e.g., gull wing), should as a minimum, have the junction of the leads with the components and the assembly coated.

26.1.1.5 Perimeter Coating Unless otherwise specified on the approved assembly drawing, the outer perimeter of assemblies should not be increased in total thickness by more than 1.0 mm as a result of conformal coating. The outer perimeter is defined as the area on each side of the board a distance of not more than 6.0 mm inward from the outer edge.

26.1.1.6 Edge Coating Unless otherwise specified on the approved assembly drawing, the dimensions of the assemblies should not be increased in length or width by more than 0.8 mm on each edge, a total of 1.5 mm by application of conformal coating.

26.1.2 Performance Guidelines The detailed guidelines for applied coatings are defined in the following paragraphs.

26.1.2.1 Thickness See Table 26-1 for the thickness for each type of conformal coating:

Table 26-1 Coating Thickness

Type AR	Acrylic Resin	0.03 - 0.13 [0.00118 to 0.00512 in]
Type ER	Epoxy Resin	0.03 - 0.13 [0.00118 to 0.00512 in]
Type UR	Urethane Resin	0.03 - 0.13 [0.00118 to 0.00512 in]
Type SR	Silicone Resin	0.05 - 0.21 [0.00197 to 0.00827 in]
Type XY	Paraxylene Resin	0.01 - 0.05 [0.000394 to 0.00197 in]

The thickness should be measured on a flat, unencumbered, cured surface of the printed wiring assembly or a coupon that has been processed with the assembly. Coupons may be of the same type of material as the printed board or may be of a nonporous material such as metal or glass. As an alternative, a wet film thickness measurement may be used to establish the coating thickness provided there is documentation that correlates the wet and dry film thickness.

26.1.2.2 Coating Coverage Conformal coating needs to be of the type specified on the assembly drawing and should be:

- Completely cured and homogeneous.
- Covered by only those areas specified on the assembly drawing.
- Free of blisters, or breaks which affect the assembly operations or sealing properties of the conformal coating.
- Free of voids, bubbles, or foreign material which expose component conductors, printed wiring conductors (including ground planes) or other conductors, and/or violate design electrical spacing.
- Contain no mealing, peeling, or wrinkle (nonadherent areas).

26.1.3 Rework of Conformal Coating Procedures that describe the removal and replacement of conformal coating need to be documented and available for review.

26.1.4 Conformal Coating Inspection Visual inspection of conformal coating may be performed without magnification. Inspection for conformal coating coverage may be performed under an ultraviolet (UV) light source when using conformal coating material containing a UV tracer. Magnification from 2X to 4X may be used for referee purposes.

26.2 Encapsulation The material specification and suppliers instructions, as applicable needs to be followed. The material needs to be used within the time period specified (both shelf life and pot life) or used within the time period indicated by a documented system the manufacturer has established to mark and control age-dated material.

26.2.1 Application The encapsulant materials needs to be continuous in all areas designated for coverage on the assembly drawing. When used, masking material should have no deleterious effect on the printed boards and should be removable without contaminant residue.

26.2.1.1 Encapsulant-Free Surfaces All portions of the assembly not designated to receive encapsulant material need to be free of any encapsulant material.

26.2.2 Performance Guidelines The applied encapsulant needs to be completely cured, homogeneous, and cover only those areas specified on the assembly drawing.

The encapsulant should be free of bubbles, blisters, or breaks that affect the printed wiring assembly operation or sealing properties of the encapsulant material. There should

be no visible cracks, crazes, mealing, peeling, and/or wrinkles in the encapsulant material.

26.2.3 Rework of Encapsulant Material Procedures that describe the removal and replacement of encapsulant material should be documented and available for review (e.g., within the manufacturers ISO 9000: 2000 documentation or equivalent written procedures).

26.2.4 Encapsulant Inspection Visual inspection of encapsulation may be performed with magnification.

27 DOCUMENTATION

The documentation package for describing component mounting requirements usually consists of a master drawing, master pattern drawing, copies of artwork (film or paper), mounting structure assembly drawing, parts list, and schematic/logic diagram. The documentation package may be provided in either hard copy or electronic data. All electronic data should meet the requirements of IPC-2510 series of standards (GenCAM).

Other documentation may include numerical control data for drilling, routing, libraries, tests, artwork, and special tooling. There are design and documentation features/ requirements that apply to the basic layout, the production master (artwork), the mounting structure itself and the end item component or printed board assembly. All must be taken into consideration during the design of the mounting structures for the bare die, through-hole, SMT or the mounting structure for the BGA and fine pitch BGA.

Documentation should meet the requirements of IPC-D-325. In order to provide the best documentation package possible, it is important to review IPC-D-325 and identify all the criteria that are affected by the design process.

27.1 Drawing Requirements During the formal design review prior to layout, special tools that can be generated by the design area in the form of artwork or numerical control data should be considered. This tooling may be needed by fabrication, assembly, or testing. Examples of such tooling are artwork overlays, artwork solder resist stripping, numerical data for automatic attachment, solder paste stencil, plots of numerical data to be used as check films.

When viewing the documentation, it is always viewed from the primary side. All phototool generation is viewed from the primary side as well. The definition of layers of the product needs to be viewed as viewing from and looking through the particular part from the primary side.

Accuracy and skill must be sufficient to eliminate inaccuracies from the layout as being interpreted during the artwork generation process. This requirement can be minimized by strictly adhering to grid systems, which define all features on the board or on the bare die.

Layout notes should be as complete as possible with the addition of appropriate notations. Marking requirements and revision status level definition is key to maintaining configuration management conditions. It is especially important for the engineering review cycle, a quoting effort, and when someone uses the document other than the originator.

27.2 Electronic Data Transfer All information about documentation is also appropriate for electronic data transmission. Since many CAD systems have their own native database, everyone is promoting some form of unique format that has a neutral concept, thus avoiding sending the native database to the suppliers.

Unfortunately, the lowest common denominator for years has been a machine language. This is trying to be circumvented by such formats as the IPC-D-350, IPC-D-356 and IPC-2510 series of documents. Archiving electronic data should be in accordance with these documents. Delivery of computer generated data, as a part of the documentation package, needs to meet the requirements stated in those packages.

With automated techniques, the database needs to detail all information that is needed to produce the printed board or mounting structure for the bare die. This includes all notes, plating requirements, board thickness, etc. The test plots should be employed to verify that the data matches the requirements.

27.3 Specifications In many instances, documentation references other specifications. These should be clear and need to be provided in this same manner in which the original package is provided (hard copy or electronic).

Conformance test circuitry should be provided, thus the part can be tested through destructive techniques. As a minimum, conformance test circuitry should include:

- Board part number/revision letter.
- Traceability identification.
- Date code.
- Manufacturer's identification e.g., commercial and government entity (CAGE) logo, etc.
- Special coding systems may be used provided they are identified on the master drawing.

27.4 Printed Board Assembly Documentation Process Flow Understanding the flow of the documentation package is important to providing the appropriate documentation for component mounting. There is direct applicability for each document in the set to cross-reference those attributes that are significant to providing quality assembly product.

Note: Figure 27-1 shows the various steps and those documents intended to control the process and the product. It should be noted that in many instances the panel used to

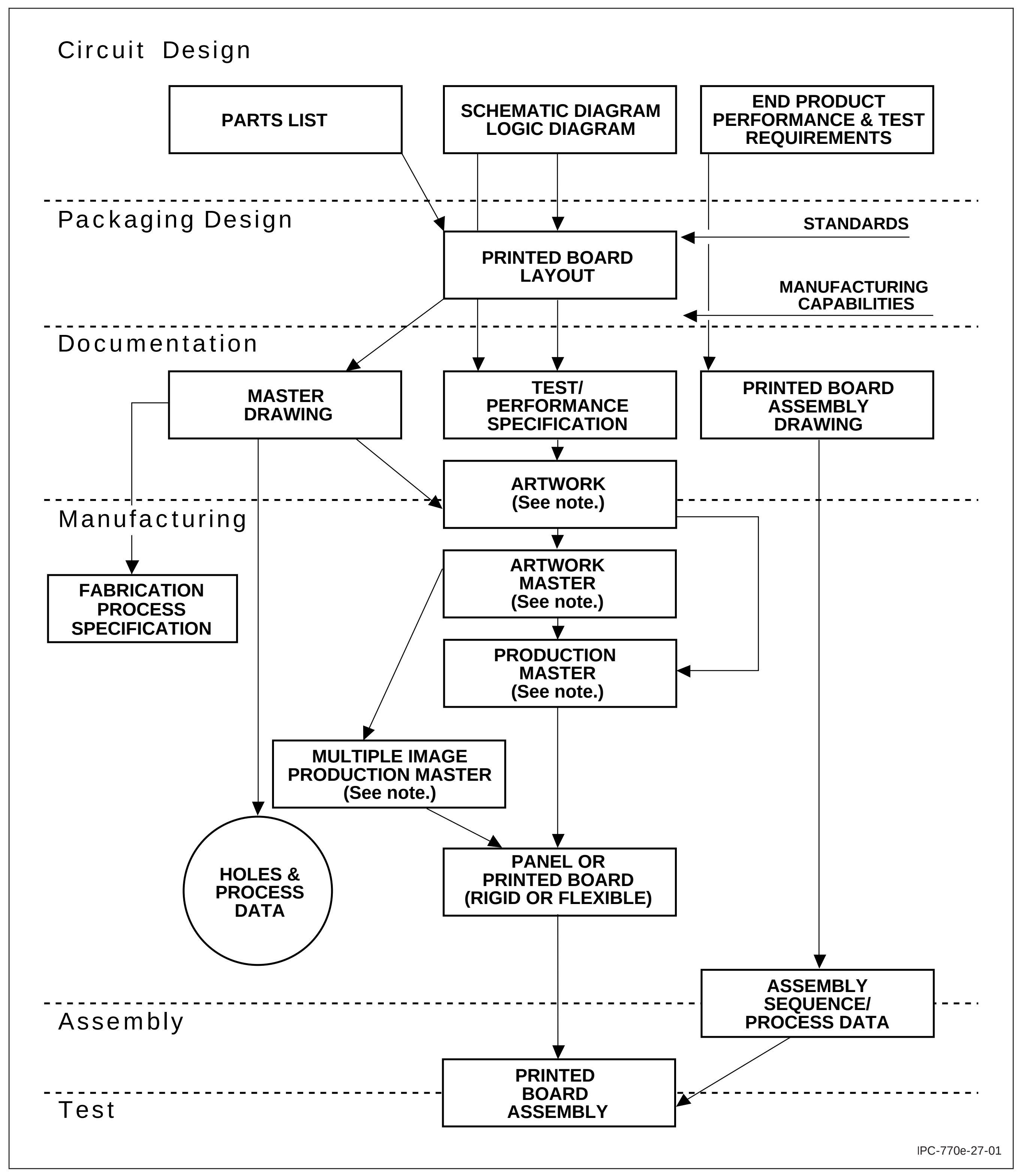
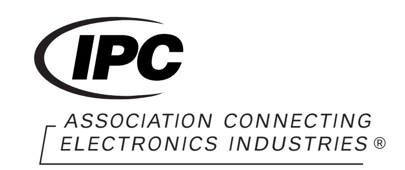


Figure 27-1 Documentation Set Flow Characteristics

assemble the boards could also be part of the documentation set. It should be noted that assembly sequencing could sometimes also be important especially if conformal coating is required as a part of the process.

27.5 Documentation for SMT Documentation used to fabricate the circuit substrate and assemble the product must be accurate and easy to understand. Details, specifications and notes guide both the assembly processing and control the quality level of a product. Unique materials or special assembly instructions, such as moisture sensitivity and handling, need to be included on the face of the detail drawings or in the documentation package.



ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847 509.9798

SUBMITTOR INFORMATION:

Name: ______

Company: ______

City: ______

State/Zip: ______

Telephone: ______

Date: ______

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: ______

Document(s) to which this term applies: ______

Committees affected by this term: ______

Office Use

IPC Office	**Committee 2-30**
Date Received: ______	Date of Initial Review: ______
Comments Collated: ______	Comment Resolution: ______
Returned for Action: ______	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: ______	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:

Committee 2-30 has approved the above term for release in the next revision.

Name: ______ Committee: IPC 2-30 Date: ______

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel 847/509-9700
fax 847/509-9798
www.ipc.org
e-mail: answers@ipc.org

IPC World Wide Web Page www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, and job opportunities. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Gencam@ipc.org

Gencam deals with issues regarding the Gencam™ standards and specifications for Printed Circuit Board Layout and Design.

LeadFree@ipc.org

This forum acts as a peer interaction resource for staying on top of lead elimination activities worldwide and within IPC.

IPC_New_Releases@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC publications, updates and standards.

ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e.<mail list> @ipc.org), as it would be distributed to all the subscribers.

Example for subscribing:
To: LISTSERV@IPC.ORG
Subject:
Message: subscribe TechNet Joseph H. Smith

Example for signing off:
To: LISTSERV@IPC.ORG
Subject:
Message: signoff DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words, if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org. Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:
To: TechNet@IPC.ORG
Subject: <your subject>
Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori
tel 847/790-5315
fax 847/504-2315
e-mail: sasako@ipc.org
www.ipc.org/html/forum.htm

Education and Training

IPC conducts local educational workshops and national conferences to help you better understand conventional and emerging technologies. Members receive discounts on registration fees. Visit www.ipc.org to see what programs are coming to your area.

IPC Certification Programs

IPC provides world-class training and certification programs based on several widely-used IPC standards, including the IPC-A-610, the J-STD-001, and the IPC-A-600. IPC-sponsored certification gives your company a competitive advantage and your workforce valuable recognition.

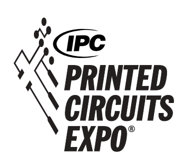
For more information on programs, contact Alexandra Curtis
tel 847/790-5377 fax 847/509-9798
e-mail: curtal@ipc.org www.ipc.org

IPC Video Tapes and CD-ROMs

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness. Members receive discounts on purchases.

For more information on IPC Video/CD Training, contact Mark Pritchard
tel 505/758-7937 ext. 202 fax 505/758-7938
e-mail: markp@ipcvideo.org www.ipc.org

IPC Printed Circuits Expo®



IPC Printed Circuits Expo is the largest trade exhibition in North America devoted to the PWB manufacturing industry. Over 90 technical presentations make up this superior technical conference. Visit www.ipcprintedcircuitexpo.org for upcoming dates and information.

Exhibitor information:
Contact: Mary MacKinnon
Sales Manager
tel 847/790-5386
e-mail: MaryMackinnon@ipc.org

Alicia Balonek
Exhibits Manager
tel 847/790-5398
e-mail: AliciaBalonek@ipc.org

Registration information:
tel 847/790-5361
fax 847/509-9798
e-mail: registration@ipc.org

APEX® / IPC SMEMA Council Electronics Assembly Process Exhibition & Conference



APEX is the premier technical conference and exhibition dedicated entirely to the electronics assembly industry. Visit www.GoAPEX.org for upcoming dates and more information.

Exhibitor information:
Contact: Mary MacKinnon
tel 847/790-5386
e-mail: MaryMacKinnon@ipc.org

Registration information:
tel 847/790-5360
fax 847/509-9798
e-mail: goapex@ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Director
tel 847/790-5309 fax 847/509-9798
e-mail: JeanetteFerdman@ipc.org www.ipc.org

Application for IPC Site Membership



Thank you for your decision to join IPC, Association Connecting Electronics Industries. IPC membership is site specific, which means that benefits of IPC membership are extended only to employees at the site that is designated on this application.

To help IPC serve your member site in the most effective manner possible, please tell us what work is being done at your site by choosing the most appropriate member category. *(Check one box only.)*

❑ INDEPENDENT PRINTED CIRCUIT BOARD MANUFACTURER

This facility manufactures, and sells to other companies, printed wiring boards (PWB's) or other electronic interconnection products on the merchant market.

What products do you make for sale?

❑ One- and two-sided rigid, multilayer printed boards ❑ Flexible printed boards ❑ Other interconnections

Site General Manager____

Name Title

❑ EMSI COMPANY - Independent Electronics Assembly

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Site General Manager____

Name Title

❑ OEM - Original Equipment Manufacturer

This facility purchases and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line?

____

Site General Manager ____

Name Title

❑ INDUSTRY SUPPLIER

This facility supplies raw materials, machinery, equipment, or services used in the manufacture or assembly of electronic interconnection products.

What products or services does your company supply? (50 word limit, please)
The information that you provide here will appear in the next edition of the IPC Membership Directory.

Our company supplies:

____

____

____

____

❑ GOVERNMENT AGENCY/ACADEMIC TECHNICAL LIAISON

This government agency or accredited university, college or technical training school is directly concerned with design, research and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Please proceed to page 2 to complete the membership application.

Application for IPC Site Membership



Site Information: (Please print or type)

Company Name

Street Address

City | State | Zip/Postal Code | Country

Main Switchboard Phone No | Main Fax No.

Company E-Mail Address | Website URL

Name of Primary Contact for all IPC matters | Title | Mail Stop

Phone No. | Fax No | E-Mail

Name of Senior Management Contact: | Title: | Mail Stop

Phone No | Fax No | E-Mail

Please attach business card of primary contact here.

Please designate your site's Technical Representatives:

For PWB/PWA design-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

For PCB fabrication-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

For Electronics Assembly-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

Please designate your site's Management Representatives:

For PWB/PWA design-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

For PCB fabrication-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

For Electronics Assembly-related information and activities:

Contact Name | Title | Phone | Fax | E-mail

Please proceed to page 3 to complete the membership application.

Application for IPC Site Membership



MEMBERSHIP DUES SCHEDULE

Please check one:

❑ **$1,000.00 –** Annual dues for Primary Site Membership
Twelve months of IPC membership begins from the time the application and payment are received at the IPC office.

❑ **$800.00 –** Annual dues for Additional Facility Membership
An additional membership for a site within an organization where there already is a current Primary Site IPC membership.

❑ **$600.00** –** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. USD
** Please provide proof of annual sales.

❑ **$250.00 –** Annual dues for Government Agency or Academic Technical Liaison Membership. Must be not-for-profit organization.

TMRC MEMBERSHIP

❑ Please send information on participation in the Technology Market Research Council (TMRC) program. Only current IPC member sites are eligible to participate in this **calendar year** program, which is available for an additional fee.

❑ **Yes, sign up our site now:**

$950.00 - Primary TMRC member site

$400.00 - Additional facility TMRC member. Another site within our organization is already a TMRC program participant.

Name of Primary Contact for all TMRC matters:

____

Phone ______________ Fax ______________

E-Mail ______________________________

PAYMENT INFORMATION

Enclosed is our check/money order for $________________________

Mail application with check or money order to:

IPC
Dept. 77-3491
Chicago, IL 60678-3491

Fax or mail application with credit card payment to:

IPC
***2215 Sanders Road**
Northbrook, IL 60062-6135
Tel: 847-509-9700
Fax: 847-509-9798
**** Overnight deliveries to this address only***

Please bill my credit card (circle one) for $________________________

❑ MasterCard ❑ American Express ❑ Visa ❑ Diners Club

Account No ______________ Expiration Date ______________

Name of Card Holder ______________________________

Authorized Signature ______________________________

Phone Number ______________________________

QUESTIONS ?

Call the IPC Member Services Department in Northbrook, Illinois, at: 847-509-9700 (extensions 5309/5372)

or fax us at 847.509-9798

E-mail: JeanetteFerdman@ipc.org SusanStorck@ipc.org

Please proceed to page 4 to complete the membership application.

Application for IPC Site Membership



INFORMATION DISTRIBUTION

IPC has significant member benefits available to a wide range of individuals within your organization. To ensure that your facility takes advantage of these benefits, please provide the name of the individual responsible for each of the functional areas listed below. If one person has multiple responsibilities, please list that person's name as many times as necessary.

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Sales/Marketing:

Name | Title/Mail Stop | Phone | Fax | E-mail

Finance (CFO)

Name | Title/Mail Stop | Phone | Fax | E-mail

Human Resources

Name | Title/Mail Stop | Phone | Fax | E-mail

Environmental/Safety

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Training

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IPC REVIEW SUBSCRIPTION LIST

One of the many benefits of IPC membership is a subscription to the IPC *Review,* our monthly magazine. Please list below the names of individuals who would benefit from receiving our magazine, which provides information about the industry, IPC news, and other items of interest. A subscription for the IPC Primary Contact person is entered automatically.

Name | Title/Mail Stop

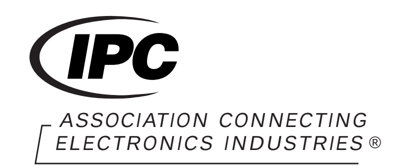
Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop

Name | Title/Mail Stop



Standard Improvement Form

IPC-CM-770E

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798
E-mail: answers@ipc.org

1. I recommend changes to the following:
   ___ Requirement, paragraph number __________
   ___ Test Method number __________, paragraph number __________

   The referenced paragraph number has proven to be:
   ___ Unclear ___ Too Rigid ___ In Error
   ___ Other ______________________________

2. Recommendations for correction:

   ____
   ____
   ____
   ____

3. Other suggestions for document improvement:

   ____
   ____
   ____
   ____

Submitted by:

Name ______________________________ Telephone ______________________________

Company ______________________________ E-mail ______________________________

Address ______________________________

City/State/Zip ______________________________ Date ______________________________



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